Everest-DEV-Board

User Guide

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1. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

1.2 Revision 1.1

Section 3.13 with UART pinout description added.

1.3 Revision 1.2

Change to hardware revision A.

2. Getting Started

2.1 Kit Contents

The Everest DEV Board Kit includes the following items.

Item	Quantity
Everest DEV Board	1
12 V / 5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for UART / power interface to PC	0
Free one-year Libero Gold software license	1

Note: The Everest DEV Board offers an on-board FlashPro5 programmer, which can be used to program and debug with Identify, SmartDebug and embedded application software using SoftConsole.

2.2 Block Diagram

The following block diagram shows all of the components of the Everest DEV Board.

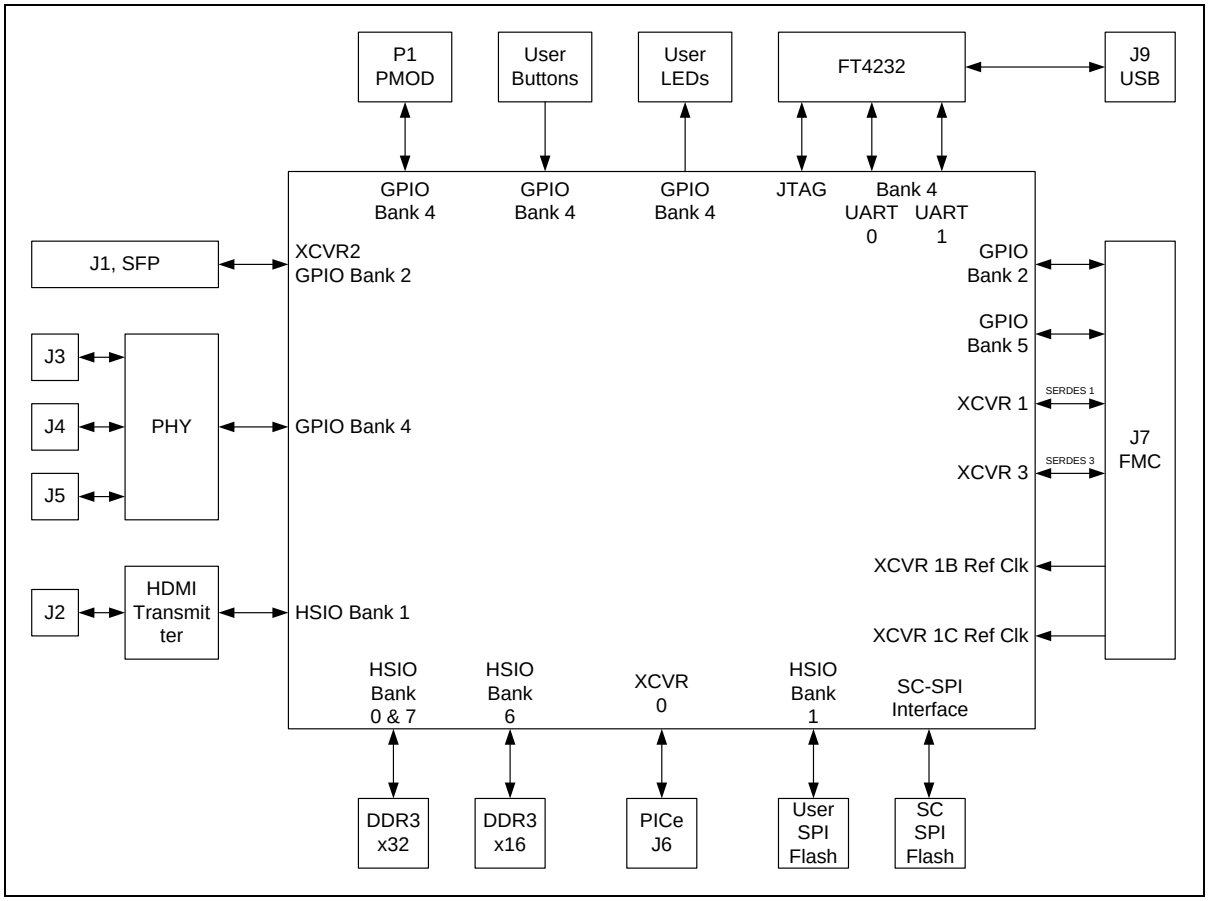

Figure 1: Everest DEV Board block diagram

2.3 Board Overview

The Everest DEV Board features the Microsemi PolarFire™ MPF300T-1FCG1152 FPGA, which offers the following capabilities:

- 20 Kb dual-port or two-port large static random-access memory (LSRAM) block with a built-in single error correct double error detect unit (SECDEC)
- 64 x 12 two-port µSRAM block implemented as an array of latches
- 18 x 18 Multiply Accumulate (MACC) block with a hardened pre-adder, a 48-bit accumulator
- Built-in µPROM, modifiable at program time, readable at run time for user data storage
- Digest integrity check for FPGA, µPROM and sNVM
- Low-power features:
  - Low device static power
  - Low inrush current
  - Low power transceivers
  - Unique Flash*Freeze (F*F) mode
  - High-performance communication interfaces

The Everest DEV Board comes with several standard interfaces like:

- VSC8575 with three RJ45 connectors for 10/100/1000 Mbps ethernet
- 8 Full-Duplex Transceiver lanes connected through FMC connector
- HPC FMC connector
- DDR3 memory
- X4 lane PCIe edge connector
- SPF+ connector
- Two SPI Flash devices (user/config)

The following labeled image highlights various components of the Everest DEV Board.

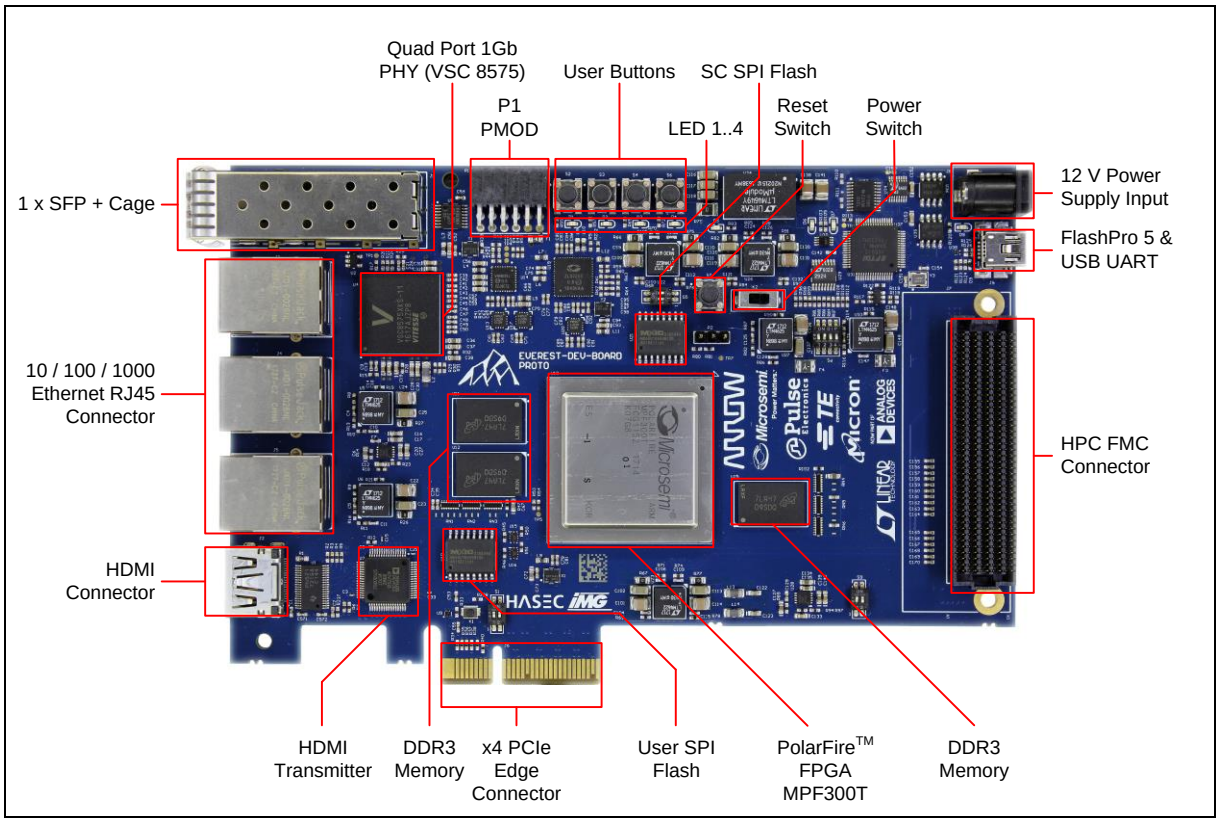

Figure 2: Components of the Everest DEV Board

The following table lists the important components of the Everest DEV Board:

Table 1: Everest DEV Board Components

component	label on board	description
featured device		
PolarFire™ FPGA		MPF300T-1FCG1152I with data security feature
power supply		
12 V power supply input	J8	The board is powered by a 12 V power source using an external +12 V / 5 A DC jack
ON/OFF switch	K2	Power ON/OFF switch from +12 V external DC jack
reset switch	S7	Push-button system reset for the PolarFire™ device
general purpose I/O		
switches	S2, S3, S4 & S6	user buttons 1 - 4

component	label on board	description
LEDs	D1, D2, D3 & D4	user LEDs 1 - 4
communication interfaces		
SFP+	J1	optical interface via one XCVR2 lane
HDMI	J2	HDMI connector
Three RJ45 ethernet jacks	J3, J4, J5	Ethernet jacks connected to the PolarFire™ device via Microsemi quad 10/100/1000 BASE-T PHY VSC8575
x4 PCIe	J6	PCIe edge connector with for XCVR0 lanes
FMC HPC	J7	FMC connector with four XCVR1, four XCVR3 lanes and GPIOs of Bank 2 and 4
USB mini B	J9	UART0 and UART1 via FT4232 interface
memory chips		
x32 DDR3	U11 & U12	Two 8Gb x16 DDR3L SDRAM devices offering 2GB
x16 DDR3	U25	One 8Gb x16 DDR3L SDRAM devices offering 1GB
user SPI-Flash	U10	128 MB user SPI-Flash
SC SPI-Flash	U21	128 MB System Config SPI-Flash
clocks		
Clock Network synchronous chip	U19	ZL30265LD multiplier and frequency synthesizer
XCVR_0A Reference Clock	J6	PCIe Reference Clock
FPGA programming and debugging		
USB mini B	J9	FlashPro 5 JTAG programmer

2.4 Compatibility with Daughter Boards

Daughter boards with an FMC connector can be plugged in to the Everest DEV Board.

2.5 Handling the Board

Pay attention to the following points while handling or operating the board:

Handle the board with electrostatic discharge (ESD) precautions to avoid damage.

For information about ESD precautions see

https://www.microsemi.com/documentportal/doc_view/126483-esd-appnote.

2.6 Board-Setup

2.6.1 Toggle-Switch S1 – PCIe

SWITCH	PCIe LANES
S1-1 (marking)	x4
S1-2	x1

2.6.2 Toggle -Switch S5 – SC SPI-Flash enable

SWITCH	SC SPI-FLASH
S5-1 (marking)	DISABLE
S5-2	ENABLE

2.6.3 DIP-Switch S8 – FMC Voltage Selector

SWITCH	FMC VOLTAGE
S8-1 off, S8-2 off	1.8 V
S8-1 on, S8-2 off	2.5 V
S8-1 off, S8-2 on	undefined (not recommended)
S8-1 on, S8-2 on	3.3 V

2.6.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

SWITCH	VDDAUX2 & VDDAUX5
S9-1 (marking)	2.5 V
S9-2	FMC voltage

2.7 Powering up the Board

Please check the correct setting of all DIP-switches before powering up the board.

The Everest DEV Board is powered up using either the 12 V DC jack or the PCIe connector.

For programming connect it although with your computer using USB mini B connector J9.

The Everest DEV Board ships with a pre-programmed LED toggling hello world design.

3. Connectors

3.1 Connector J1 – 10GBit Ethernet

Table 1: pin assignment J1

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
1				GND, VEET
2				TX_FAULT
3				TX_DIS
4				SDA/MDEF2
5				SCL/MDEF1
6				MOD/MDEF0
7				RS0
8				RX_LOS
9				RS1
10				GND, VEER
11				GND, VEER
12	AD30	XCVR_2_RX1_N	SERDES-2	RD-
13	AD29	XCVR_2_RX1_P	SERDES-2	RD+
14				GND, VEER
15				VCCR
16				VCCT
17				GND, VEET
18	AE31	XCVR_2_TX1_P	SERDES-2	TD+
19	AE32	XCVR_2_TX1_N	SERDES-2	TD-
20				GND, VEET
Shield				SGND

3.2 Connector J2 – HDMI

Table 2: pin assignment J2

PIN	SIGNAL	PIN	SIGNAL
1	HDMI_TX2_P	**11**	GND
2	GND	**12**	HDMI_TXC_N
3	HDMI_TX2_N	**13**	CEC_CONN
4	HDMI_TX1_P	**14**	NC
5	GND	**15**	HDMI_CONN_SCL
6	HDMI_TX1_N	**16**	HDMI_CONN_SDA
7	HDMI_TX0_P	**17**	GND
8	GND	**18**	5V_HDMI_OUT
9	HDMI_TX0_N	**19**	HOT_PLUG_CONN
10	HDMI_TXC_P		

3.3 Connector J3 – 1GBit Ethernet

Table 3: pin assignment J3

PIN	SIGNAL	PIN	SIGNAL
P1	PRI_COM	**P9**	TD3-
P2	TD0+	**P10**	NC
P3	TD0-	**P11**	LEDG+
P4	TD1+	**P12**	LEDG-
P5	TD1-	**P13**	LEDY+
P6	TD2+	**P14**	LEDY-
P7	TD2-	**P15**	SGND
P8	TD3+	**P16**	SGND

3.4 Connector J4 – 1GBit Ethernet

Table 4: pin assignment J4

PIN	SIGNAL	PIN	SIGNAL
P1	PRI_COM	**P9**	TD3-
P2	TD0+	**P10**	NC
P3	TD0-	**P11**	LEDG+
P4	TD1+	**P12**	LEDG-
P5	TD1-	**P13**	LEDY+
P6	TD2+	**P14**	LEDY-
P7	TD2-	**P15**	SGND
P8	TD3+	**P16**	SGND

3.5 Connector J5 – 1GBit Ethernet

Table 5: pin assignment J5

PIN	SIGNAL	PIN	SIGNAL
P1	PRI_COM	**P9**	TD3-
P2	TD0+	**P10**	NC
P3	TD0-	**P11**	LEDG+
P4	TD1+	**P12**	LEDG-
P5	TD1-	**P13**	LEDY+
P6	TD2+	**P14**	LEDY-
P7	TD2-	**P15**	SGND
P8	TD3+	**P16**	SGND

3.6 Connector J6 – x4 PCIe

3.6.1 J6A

Table 6: pin assignment J6A

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
A1				PRSNT1#
A2				+12V
A3				+12V
A4				GND
A5				TCK
A6				TDI
A7				TDO
A8				TMS
A9				+3V3
A10				+3V3
A11				PERST#
A12				GND
A13	W27	XCVR_0A_REFCLK_P	SERDES-0	REFCLK+
A14	W28	XCVR_0A_REFCLK_N	SERDES-0	REFCLK-
A15				GND
A16	V33	XCVR_0_TX0_P	SERDES-0	PER0_P
A17	V34	XCVR_0_TX0_N	SERDES-0	PER0_N
A18				GND
A19				RSVD
A20				GND
A21	Y33	XCVR_0_TX1_P	SERDES-0	PER1_P
A22	Y34	XCVR_0_TX1_N	SERDES-0	PER1_N
A23				GND
A24				GND
A25	AA31	XCVR_0_TX2_P	SERDES-0	PER2_P
A26	AA32	XCVR_0_TX2_N	SERDES-0	PER2_N
A27				GND
A28				GND
A29	AB33	XCVR_0_TX3_P	SERDES-0	PER3_P
A30	AB34	XCVR_0_TX3_N	SERDES-0	PER3_N
A31				GND
A32				RSVD

3.6.2 J6B

Table 7: pin assignment J6B

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
B1				+12V
B2				+12V
B3				+12V
B4				GND
B5	AD23	HSIO85NB1	BANK-1	SMCLK
B6	AD25	HSIO84NB1	BANK-1	SMDAT
B7				GND
B8				+3V3
B9				TRST#
B10				+3V3aux
B11	AF24	HSIO86PB1	BANK-1	WAKE#
B12				RSVD
B13				GND
B14	V29	XCVR_0_RX0_P	SERDES-0	PET0_P
B15	V30	XCVR_0_RX0_N	SERDES-0	PET0_N
B16				GND
B17				PRSNT2#
B18				GND
B19	W31	XCVR_0_RX1_P	SERDES-0	PET1_P
B20	W32	XCVR_0_RX1_N	SERDES-0	PET1_N
B21				GND
B22				GND
B23	Y29	XCVR_0_RX2_P	SERDES-0	PET2_P
B24	Y30	XCVR_0_RX2_N	SERDES-0	PET2_N
B25				GND
B26				GND
B27	AB29	XCVR_0_RX3_P	SERDES-0	PET3_P
B28	AB30	XCVR_0_RX3_N	SERDES-0	PET3_N
B29				GND
B30				RSVD
B31				PRSNT2#
B32				GND

3.7 Connector J7 – FMC HPC

3.7.1 J7A

Table 8: pin assignment J7A

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
A1				GND1
A2	P29	XCVR_1_RX1_P	SERDES-1	DP1_M2C_P
A3	P30	XCVR_1_RX1_N	SERDES-1	DP1_M2C_N
A4				GND2
A5				GND3
A6	R31	XCVR_1_RX2_P	SERDES-1	DP2_M2C_P
A7	R32	XCVR_1_RX2_N	SERDES-1	DP2_M2C_N
A8				GND4
A9				GND5
A10	T29	XCVR_1_RX3_P	SERDES-1	DP3_M2C_P
A11	T30	XCVR_1_RX3_N	SERDES-1	DP3_M2C_N
A12				GND6
A13				GND7
A14	G31	XCVR_3_RX0_P	SERDES-3	DP4_M2C_P
A15	G32	XCVR_3_RX0_N	SERDES-3	DP4_M2C_N
A16				GND8
A17				GND9
A18	J31	XCVR_3_RX1_P	SERDES-3	DP5_M2C_P
A19	J32	XCVR_3_RX1_N	SERDES-3	DP5_M2C_N
A20				GND10
A21				GND11
A22	P33	XCVR_1_TX1_P	SERDES-1	DP1_ C2M _P
A23	P34	XCVR_1_TX1_N	SERDES-1	DP1_ C2M _N
A24				GND12
A25				GND13
A26	T33	XCVR_1_TX2_P	SERDES-1	DP2_ C2M_P
A27	T34	XCVR_1_TX2_N	SERDES-1	DP2_ C2M_N
A28				GND14
A29				GND15
A30	U31	XCVR_1_TX3_P	SERDES-1	DP3_ C2M_P
A31	U32	XCVR_1_TX3_N	SERDES-1	DP3_ C2M_N
A32				GND16
A33				GND17
A34	F33	XCVR_3_TX0_P	SERDES-3	DP4_ C2M_P
A35	F34	XCVR_3_TX0_N	SERDES-3	DP4_ C2M_N
A36				GND18
A37				GND19
A38	H33	XCVR_3_TX1_P	SERDES-3	DP5_ C2M_P
A39	H34	XCVR_3_TX1_N	SERDES-3	DP5_ C2M_N
A40				GND20

3.7.2 J7B

Table 9: pin assignment J7B

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
B1				RES1, NC
B2				GND21
B3				GND22
B4	L27	XCVR_1C_REFCLK_P	SERDES EXT REF CLK	DP9_M2C_P
B5	L28	XCVR_1C_REFCLK_N	SERDES EXT REF CLK	DP9_M2C_N
B6				GND23
B7				GND24
B8	R27	XCVR_1B_REFCLK_P	SERDES EXT REF CLK	DP8_M2C_P
B9	R28	XCVR_1B_REFCLK_N	SERDES EXT REF CLK	DP8_M2C_N
B10				GND25
B11				GND26
B12	L31	XCVR_3_RX3_P	SERDES-3	DP7_M2C_P
B13	L32	XCVR_3_RX3_N	SERDES-3	DP7_M2C_N
B14				GND27
B15				GND28
B16	K29	XCVR_3_RX2_P	SERDES-3	DP6_M2C_P
B17	K30	XCVR_3_RX2_N	SERDES-3	DP6_M2C_N
B18				GND29
B19				GND30
B20	J27	XCVR_3A_REFCLK_P	SERDES-3	GBTCLK1_M2C_P
B21	J28	XCVR_3A_REFCLK_N	SERDES-3	GBTCLK1_M2C_N
B22				GND31
B23				GND32
B24				DP9_C2M_P
B25				DP9_C2M_N
B26				GND33
B27				GND34
B28	H29	XCVR_3C_REFCLK_P	SERDES EXT REF CLK	DP8_C2M_P
B29	H30	XCVR_3C_REFCLK_N	SERDES EXT REF CLK	DP8_C2M_N
B30				GND35
B31				GND36
B32	M33	XCVR_3_TX3_P	SERDES-3	DP7_C2M_P
B33	M34	XCVR_3_TX3_N	SERDES-3	DP7_C2M_N
B34				GND37
B35				GND38
B36	K33	XCVR_3_TX2_P	SERDES-3	DP6_C2M_P
B37	K34	XCVR_3_TX2_N	SERDES-3	DP6_C2M_N
B38				GND39
B39				GND40
B40				RES0, NC

3.7.3 J7C

Table 10: pin assignment J7C

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
C1				GND41
C2	N31	XCVR_1_TX0_P	SERDES-1	DP0_C2M_P
C3	N32	XCVR_1_TX0_N	SERDES-1	DP0_C2M_N
C4				GND42
C5				GND43
C6	M29	XCVR_1_RX0_P	SERDES-1	DP0_M2C_P
C7	M30	XCVR_1_RX0_N	SERDES-1	DP0_M2C_N
C8				GND44
C9				GND45
C10	F14	GPIO19PB2	BANK-2	LA06_P
C11	F15	GPIO19NB2	BANK-2	LA06_N
C12				GND46
C13				GND47
C14	G10	GPIO21PB2	BANK-2	LA10_P
C15	F10	GPIO21NB2	BANK-2	LA10_N
C16				GND48
C17				GND49
C18	B9	GPIO25PB2	BANK-2	LA14_P
C19	A9	GPIO25NB2	BANK-2	LA14_N
C20				GND50
C21				GND51
C22	G4	GPIO244PB2 / CCC_SW_CLKIN_S_0	BANK-2	LA18_P_CC
C23	F4	GPIO244NB2	BANK-2	LA18_N_CC
C24				GND52
C25				GND53
C26	J11	GPIO04PB2	BANK-2	LA27_P
C27	H11	GPIO04NB2	BANK-2	LA27_N
C28				GND54
C29				GND55
C30	T7	GPIO218PB4	BANK-4	SCL
C31	T8	GPIO218NB4	BANK-4	SDA
C32				GND56
C33				GND57
C34				GA0, GND
C35	FMC_12V_C2M			12P0V_1
C36				GND58
C37	FMC_12V_C2M			12P0V_2
C38				GND59
C39	FMC_3V3_C2M			3P3V_1
C40				GND60

3.7.4 J7D

Table 11: pin assignment J7D

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
D1	V14	GPIO207PB4	BANK-4	PG_C2M
D2				GND61
D3				GND62
D4	N27	XCVR_1_A_REFCLK_P	SERDES-1	GBTCLK0_M2C_P
D5	N28	XCVR_1_A_REFCLK_N	SERDES-1	GBTCLK0_M2C_N
D6				GND63
D7				GND64
D8	E1	GPIO245PB2 / CCC_SW_CLKIN_S_1	BANK-2	LA01_P_CC
D9	D1	GPIO245NB2	BANK-2	LA01_N_CC
D10				GND65
D11	H14	GPIO3PB2	BANK-2	LA05_P
D12	G14	GPIO3NB2	BANK-2	LA05_N
D13				GND66
D14	G12	GPIO18PB2	BANK-2	LA09_P
D15	G11	GPIO18NB2	BANK-2	LA09_N
D16				GND67
D17	G9	GPIO6PB2 / CLKIN_S_4	BANK-2	LA13_P
D18	F9	GPIO6NB2	BANK-2	LA13_N
D19				GND68
D20	F8	GPIO9PB2 / CLKIN_S_6	BANK-2	LA17_P_CC
D21	F7	GPIO9NB2	BANK-2	LA17_N_CC
D22				GND69
D23	B5	GPIO255PB2	BANK-2	LA23_P
D24	A5	GPIO255NB2	BANK-2	LA23_N
D25				GND70
D26	H7	GPIO8PB2 / DQS	BANK-2	LA26_P
D27	G7	GPIO8NB2 / DQS	BANK-2	LA26_N
D28				GND71
D29				TCK, NC
D30				TDI
D31				TDO
D32	FMC_3V3_C2M			3P3VAUX
D33				TMS
D34				TRST_L
D35				GA1, GND
D36	FMC_3V3_C2M			3P3V_2
D37				GND72
D38	FMC_3V3_C2M			3P3V_3
D39				GND73
D40	FMC_3V3_C2M			3P3V_4

3.7.5 J7E

Table 12: pin assignment J7E

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
E1				GND74
E2	K18	GPIO35PB2 / CCC_SE_CLKIN_S_11	BANK-2	HA01_P_CC
E3	K17	GPIO35NB2	BANK-2	HA01_N_CC
E4				GND75
E5				GND76
E6	H16	GPIO32PB2 / DQS	BANK-2	HA05_P
E7	H17	GPIO32NB2 / DQS	BANK-2	HA05_N
E8				GND77
E9	R7	GPIO226PB5	BANK-5	HA09_P
E10	R8	GPIO226NB5	BANK-5	HA09_N
E11				GND78
E12	L8	GPIO236PB5	BANK-5	HA13_P
E13	L7	GPIO236NB5	BANK-5	HA13_N
E14				GND79
E15				HA16_P
E16				HA16_N
E17				GND80
E18				HA20_P
E19				HA20_N
E20				GND81
E21	K5	GPIO232PB5	BANK-5	HB03_P
E22	L5	GPIO232NB5	BANK-5	HB03_N
E23				GND82
E24	R5	GPIO227PB5	BANK-5	HB05_P
E25	R6	GPIO227NB5	BANK-5	HB05_N
E26				GND83
E27	P6	GPIO229PB5 / DQS	BANK-5	HB09_P
E28	P5	GPIO229NB5 / DQS	BANK-5	HB09_N
E29				GND84
E30	N4	GPIO224PB5	BANK-5	HB13_P
E31	N3	GPIO224NB5	BANK-5	HB13_N
E32				GND85
E33				HB19_P
E34				HB19_N
E35				GND86
E36				HB21_P
E37				HB21_N
E38				GND87
E39	FMC_VADJ_C2M			VADJ_1
E40				GND88

3.7.6 J7F

Table 13: pin assignment J7F

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
F1	W14	GPIO207NB4	BANK-4	PG_M2C
F2				GND89
F3				GND90
F4	J18	GPIO33PB2 / CCC_SE_CLKIN_S_10	BANK-2	HA00_P_CC
F5	J19	GPIO33NB2	BANK-2	HA00_N_CC
F6				GND91
F7	K15	GPIO0PB2	BANK-2	HA04_P
F8	J15	GPIO0NB2	BANK-2	HA04_N
F9				GND92
F10	J8	GPIO237PB5	BANK-5	HA08_P
F11	K8	GPIO237NB5	BANK-5	HA08_N
F12				GND93
F13	K7	GPIO233PB5	BANK-5	HA12_P
F14	K6	GPIO233NB5	BANK-5	HA12_N
F15				GND94
F16				HA15_P
F17				HA15_N
F18				GND95
F19				HA19_P
F20				HA19_N
F21				GND96
F22	J6	GPIO235PB5 / DQS	BANK-5	HB02_P
F23	J5	GPIO235NB5 / DQS	BANK-5	HB02_N
F24				GND97
F25	L3	GPIO223PB5 / DQS	BANK-5	HB04_P
F26	L2	GPIO223NB5 / DQS	BANK-5	HB04_N
F27				GND98
F28	N7	GPIO228PB5	BANK-5	HB08_P
F29	N6	GPIO228NB5	BANK-5	HB08_N
F30				GND99
F31	P4	GPIO222PB5	BANK-5	HB12_P
F32	P3	GPIO222NB5	BANK-5	HB12_N
F33				GND100
F34				HB16_P
F35				HB16_N
F36				GND101
F37				HB20_P
F38				HB20_N
F39				GND102
F40	FMC_VADJ_C2M			VADJ_2

3.7.7 J7G

Table 14: pin assignment J7G

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
G1				GND103
G2	F2	GPIO246PB2 / DQS / CCC_SW_PLL1_OUT0	BANK-2	CLK1_M2C_P
G3	E2	GPIO246NB2	BANK-2	CLK1_M2C_N
G4				GND104
G5				GND105
G6	C11	GPIO29PB2 / CLKIN_S_9 / CCC_SE_ CLKIN_S_9	BANK-2	LA00_P_CC
G7	B11	GPIO29NB2	BANK-2	LA00_N_CC
G8				GND106
G9	H13	GPIO1PB2	BANK-2	LA03_P
G10	H12	GPIO1NB2	BANK-2	LA03_N
G11				GND107
G12	F13	GPIO22PB2	BANK-2	LA08_P
G13	E13	GPIO22NB2	BANK-2	LA08_N
G14				GND108
G15	D9	GPIO24PB2	BANK-2	LA12_P
G16	C9	GPIO24NB2	BANK-2	LA12_N
G17				GND109
G18	B10	GPIO28PB2	BANK-2	LA16_P
G19	A10	GPIO28NB2	BANK-2	LA16_N
G20				GND110
G21	C7	GPIO12PB2	BANK-2	LA20_P
G22	B7	GPIO12NB2	BANK-2	LA20_N
G23				GND111
G24	B4	GPIO253PB2	BANK-2	LA22_P
G25	A4	GPIO253NB2	BANK-2	LA22_N
G26				GND112
G27	C3	GPIO254PB2	BANK-2	LA25_P
G28	C4	GPIO254NB2	BANK-2	LA25_N
G29				GND113
G30	D8	GPIO14PB2 / DQS	BANK-2	LA29_P
G31	C8	GPIO14NB2 / DQS	BANK-2	LA29_N
G32				GND114
G33	E7	GPIO15PB2	BANK-2	LA31_P
G34	E8	GPIO15NB2	BANK-2	LA31_N
G35				GND115
G36	G5	GPIO11PB2 / CLKIN_S_7	BANK-2	LA33_P
G37	F5	GPIO11NB2	BANK-2	LA33_N
G38				GND116
G39	FMC_VADJ_C2M			VADJ_3
G40				GND117

3.7.8 J7H

Table 15: pin assignment J7H

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
H1	FMC_VREF_A_M2C			VREF_A_M2C
H2	AA14	GPIO188PB4	BANK-4	PRSNT_M2C_L
H3				GND118
H4	F3	GPIO247PB2 / CCC_SW_CLKIN_S_2 / CCC_SW_PLL1_OUT0	BANK-2	CLK0_M2C_P
H5	E3	GPIO247NB2	BANK-2	CLK0_M2C_N
H6				GND119
H7	J14	GPIO2PB2 / DQS	BANK-2	LA02_P
H8	J13	GPIO2NB2 / DQS	BANK-2	LA02_N
H9				GND120
H10	F12	GPIO23PB2	BANK-2	LA04_P
H11	E12	GPIO23NB2	BANK-2	LA04_N
H12				GND121
H13	E10	GPIO20PB2 / DQS	BANK-2	LA07_P
H14	E11	GPIO20NB2 / DQS	BANK-2	LA07_N
H15				GND122
H16	D10	GPIO26PB2 / DQS	BANK-2	LA11_P
H17	D11	GPIO26NB2 / DQS	BANK-2	LA11_N
H18				GND123
H19	A7	GPIO16PB2	BANK-2	LA15_P
H20	A8	GPIO16NB2	BANK-2	LA15_N
H21				GND124
H22	C6	GPIO17PB2	BANK-2	LA19_P
H23	B6	GPIO17NB2	BANK-2	LA19_N
H24				GND125
H25	A2	GPIO251PB2	BANK-2	LA21_P
H26	A3	GPIO251NB2	BANK-2	LA21_N
H27				GND126
H28	H9	GPIO7PB2 / CLKIN_S_5	BANK-2	LA24_P
H29	H8	GPIO7NB2	BANK-2	LA24_N
H30				GND127
H31	E6	GPIO13PB2	BANK-2	LA28_P
H32	D6	GPIO13NB2	BANK-2	LA28_N
H33				GND128
H34	C2	GPIO252PB2 / DQS	BANK-2	LA30_P
H35	B2	GPIO252NB2 / DQS	BANK-2	LA30_N
H36				GND129
H37	C1	GPIO250PB2	BANK-2	LA32_P
H38	B1	GPIO250NB2	BANK-2	LA32_N
H39				GND130
H40	FMC_VADJ_C2M			VADJ_4

3.7.9 J7J

Table 16: pin assignment J7J

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
K1	FMC_VREF_A_M2C			VREF_B_M2C
K2				GND146
K3				GND147
K4	J1	GPIO239PB5 / CLKIN_W_2 / CCC_SW_CLKIN_W_2 / CC_SW_PLL0_OUT0	BANK-5	CLK2_M2C_P
K5	K1	GPIO239NB5	BANK-5	CLK2_M2C_N
K6				GND148
K7	L19	GPIO34PB2	BANK-2	HA02_P
K8	L18	GPIO34NB2	BANK-2	HA02_N
K9				GND149
K10	L17	GPIO30PB2	BANK-2	HA06_P
K11	M17	GPIO30NB2	BANK-2	HA06_N
K12				GND150
K13	N8	GPIO231PB5	BANK-5	HA10_P
K14	M7	GPIO231NB5	BANK-5	HA10_N
K15				GND151
K16				HA17_P_CC, NC
K17				HA17_N_CC, NC
K18				GND152
K19				HA21_P
K20				HA21_N
K21				GND153
K22				HA23_P
K23				HA23_N
K24				GND154
K25	H4	GPIO242PB5	BANK-5	HB00_P_CC
K26	H3	GPIO242NB5	BANK-5	HB00_N_CC
K27				GND155
K28	H2	GPIO240PB5 / CLKIN_W_1/CCC_SW_CLKIN_W_1	BANK-5	HB06_P_CC
K29	H1	GPIO240NB5	BANK-5	HB06_N_CC
K30				GND156
K31	N2	GPIO220PB5	BANK-5	HB10_P
K32	N1	GPIO220NB5	BANK-5	HB10_N
K33				GND157
K34				HB14_P
K35				HB14_N
K36				GND158
K37				HB17_P_CC
K38				HB17_N_CC
K39				GND159
K40	FMC_VADJ_C2M			VOI_B_M2C_2

3.7.10 J7I

Table 17: pin assignment J7I

PIN	MPF300TS-1FCG1152 PIN			SIGNAL
J1				GND131
J2	J4	GPIO241PB5 / DQS / CCC_SW_PLL0_OUT0	BANK-5	CLK3_M2C_P
J3	J3	GPIO241NB5	BANK-5	CLK3_M2C_N
J4				GND132
J5				GND133
J6	J16	GPIO31PB2	BANK-2	HA03_P
J7	K16	GPIO31NB2	BANK-2	HA03_N
J8				GND134
J9	G15	GPIO5PB2	BANK-2	HA07_P
J10	G16	GPIO5NB2	BANK-2	HA07_N
J11				GND135
J12	P9	GPIO230PB5	BANK-5	HA11_P
J13	P8	GPIO230NB5	BANK-5	HA11_N
J14				GND136
J15				HA14_P
J16				HA14_N
J17				GND137
J18				HA18_P
J19				HA18_N
J20				GND138
J21				HA22_P
J22				HA22_N
J23				GND139
J24	L4	GPIO225PB5	BANK-5	HB01_P
J25	M4	GPIO225NB5	BANK-5	HB01_N
J26				GND140
J27	M2	GPIO221PB5	BANK-5	HB07_P
J28	M1	GPIO221NB5	BANK-5	HB07_N
J29				GND141
J30	M6	GPIO234PB5	BANK-5	HB11_P
J31	M5	GPIO234NB5	BANK-5	HB11_N
J32				GND142
J33				HB15_P
J34				HB15_N
J35				GND143
J36				HB18_P
J37				HB18_N
J38				GND144
J39	FMC_VADJ_C2M			VOI_B_M2C_1
J40				GND145

3.8 Connector J8 – Power Jack

Table 18: pin assignment J8

PIN number	Signal
1	12V_Main
2	GND
3	GND

3.9 Connector J9 – USB

Table 19: pin assignment J9

PIN number	Signal
1	VB
2	D-
3	D+
4	ID, NC
5	G1, GND
6	GND
7	GND
8	GND

3.10 Connector P1 – PMOD

Table 20: pin assignment P1

PIN number	MPF300TS-1FCG1152 PIN			Signal
1	AA3	GPIO190PB4	BANK-4	IO1
2	AB5	GPIO182PB4	BANK-4	IO2
3	AA5	GPIO191NB4	BANK-4	IO3
4	W4	GPIO193PB4 / DQS	BANK-4	IO4
5				GND
6				VCC
7	AA4	GPIO191PB4	BANK-4	IO7
8	AB6	GPIO179NB4	BANK-4	IO8
9	V3	GPIO208PB4	BANK-4	IO9
10	V4	GPIO208NB4	BANK-4	IO10
11				GND
12				VCC

3.11 Connector P2 – PROBES

Table 21: pin assignment P2

PIN	MPF300TS-1FCG1152 PIN	SIGNAL
1		GND
2	G6, GPIO10NB2/LPRB_B	PROBE B
3	H6, GPIO10PB2/LPRB_A	PROBE A

3.12 LED, Push Button

Table 22: LED, Push Button

NAME	MPF300TS-1FCG1152 PIN			SIGNAL
S2	T4	GPIO217NB4 / DQS	BANK-4	PB1
S3	Y8	GPIO199NB4 / DQS	BANK-4	PB2
S4	V8	GPIO198PB4	BANK-4	PB3
S6	W10	GPIO200PB4	BANK-4	PB4
5	U11	GPIO206NB4	BANK-4	LED1
6	T5	GPIO217PB4 / DQS	BANK-4	LED2
7	W8	GPIO199PB4 / DQS	BANK-4	LED3
8	W9	GPIO201NB4	BANK-4	LED4
9	T3	GPIO209PB4	BANK-4	USER_RESET

3.13 UART

Table 23: UART

NAME	MPF300TS-1FCG1152 PIN			SIGNAL
UART0_RX	U7	GPIO218NB4	BANK-4	UART0_FTDI2PF
UART0_TX	V9	GPIO201PB4	BANK-4	UART0_PF2FTDI
UART1_RX	AA9	GPIO189NB4	BANK-4	UART1_FTDI2PF
UART1_TX	W5	GPIO195PB4	BANK-4	UART1_PF2FTDI