

Everest-MIPI CSI-2 - Demo

Getting Started

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1. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Updated for Libero 12.4.

1.2 Revision 1.0

Revision 1.0 is the first publication of this document.

2. Getting Started

This demo design includes a video and imaging demo using the PolarFire Everest DEV Board and Video MIPI CSI-2 Daughter Card. Using the on board HDMI port to print a Full HD (1920x1080@60Hz) on a HDMI monitor.

Prerequisites

For the Everest MIPC-CSI-2 Demo the following is needed:

Item	Quantity
Everest DEV Board	1
12 V / 5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for	1
UART / Programming interface to PC	
HDMI cable	1
HDMI monitor (1920x1080@60Hz)	1
MIPI CSI-2 Daughter Card	1
Image sensor module LI-AR0330-MIPI v1.1	1
Image sensor ribbon cable	1
Free one-year Libero Silver software license	1

Note 1: The Everest DEV Board offers an on-board FlashPro5 programmer, which can be used to program and debug with Identify, SmartDebug and embedded application software using SoftConsole.

Note 2: The descripted design is suitable for Everest Dev Board Rev PROTO, A and B.

2.1 Handling the Board

Pay attention to the following points while handling or operating the board:

Handle the board with electrostatic discharge (ESD) precautions to avoid damage.

For information about ESD precautions see

https://www.microsemi.com/documentportal/doc_view/126483-esd-appnote.

2.2 Board-Setup Revision PROTO

2.2.1 Toggle-Switch S1 – PCIe

Warning: S1-1 and S1-2 must not be at position on at the same time!

SWITCH ON	PCIe LANES
S1-1	x1
S1-2	x4

2.2.2 Toggle -Switch S5 – SC SPI-Flash enable

Warning: S5-1 and S5-2 must not be at position on at the same time!

SWITCH ON	SC SPI-FLASH
S5-1	ENABLE
S5-2	DISABLE

2.2.3 DIP-Switch S8 – FMC Voltage Selector

Warning: S8-1 to S8-4 must not be at position on at the same time!

SWITCH ON	FMC VOLTAGE
S8-1	3.3 V
S8-2	2.5 V
S8-3	1.8 V
S8-4	undefined (not connected)

2.2.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

Warning: S9-1 and S9-2 must not be at position on at the same time!

SWITCH ON	VDDAUX2 & VDDAUX5
S9-1	2.5 V
S9-2	FMC voltage

Use the marked settings for the demo.

2.3 Board-Setup Revision A and B

2.3.1 Toggle-Switch S1 – PCle

SWITCH	PCIe LANES
S1-1 (marking)	x4
S1-2	x1

2.3.2 Toggle -Switch S5 – SC SPI-Flash enable

SWITCH	SC SPI-FLASH
S5-1 (marking)	DISABLE
S5-2	ENABLE

2.3.3 DIP-Switch S8 – FMC Voltage Selector

SWITCH	FMC VOLTAGE
S8-1 off, S8-2 off	1.8 V
S8-1 on, S8-2 off	2.5 V
S8-1 off, S8-2 on	undefined (not recommended)
S8-1 on, S8-2 on	3.3 V

2.3.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

SWITCH	VDDAUX2 & VDDAUX5
S9-1 (marking)	2.5 V
S9-2	FMC voltage

Use the marked settings for the demo.

User Guide



Figure 1: Everest Board + MIPI CSI-2 Daughter Card

2.4 Powering up the Board

The Everest DEV Board is powered up using either the 12 V DC jack or the PCIe connector. For programming connect it although with your computer using USB mini B connector J9. A HDMI monitor should be connected with an appropriate cable via HDMI connector J2.

3. Demo Design

3.1 Prerequisites

Table 1: Software

Software	Version
Libero SoC PolarFire	V12.0
Synplify Pro	L2017.09M-SP1-1
FlashPro PolarFire	V2.0

Download the Video Demo GUI from

http://soc.microsemi.com/download/rsc/?f=mpf_dg0807_liberosocpolarfirev2p0_gui

Before you start you have to make sure, that all cores are downloaded to your local vault.

3.2 Design Implementation

The design is already fully implemented and ready to be programmed on the Everest Board. The board has to be connected with the power supply and to the PC with the USB cable. All drivers have to be installed (which should happen automatically when plugged in the first time) To program the design, there are two possibilities:

- Programming via Libero PolarFire SoC: Programming is started with the "Run PROGRAM Action" Button in the Design Flow Pane
- Programming via FlashPro Software: There is a STAPL-File ("<Design Directory>\designer\PF_AR0330_CAM_TOP\export\PF_AR0330_CAM_TOP_ADV.st p") which can be programmed with the FlashPro Software. A new FlashPro project has to be generated and the programming file loaded into.

3.3 IP Core Configuration

3.3.1 Smart Design PF_AR0330_CAM_TOP

3.3.1.1 IP Core PF_CCC_2_0

Clock Conditioning Circuitry (CCC)				
Microsemi5gCore:PF_CCC:2.2.100				
Configuration PLL-Single				
Input Frequency 50 MHz Backup Clock Bandwidth High Backup Clock Bandwidth Backup Line Backu				
C Reference Clock Delay C Feedback Clock Delay Delay Steps: 1	PF_ -REF_QK_0 P	CCC_0 OUTO_FAB OUTI_FAB PLL_LC F_CCC	2K.0- 2K.0- XX.0-	
Power / Jitter Maximize VCO for Lowest Jitter VCO = 3999.98 MHz Minimize VCO for Lowest Power		_		
Feedback Mode Post-VCO				
og	_Symbol_/			
Help x			Can	el

Figure 2: PF_CCC_2_0 Clock Options PLL

Configurator Clock Conditioning Circuitry (CCC) Aicrosemi:SgCore:PF_CCC:2.2.100	- 0
Configuration PLL-Single Clock Options PLL Output Clocks For best results, put the highest frequency first. Output Clock 0 Fenabled Requested Frequency 166.666 MHz C Actual Lower 166.666 MHz C Actual Higher 166.666 MHz Requested Phase 0 Degrees C Actual Lower 0 Degrees Actual Higher 0 Degrees Dynamic Phase Shifting Expose Enable Port Enable Bypass REF_PREDIV	
Image: Global Clock Global Clock (Gated) HS I/O Clock Dedicated Clock Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Global Clock 1 Image: Gl	PF_CCC_0
Image: Dynamic Phase Shifting Image: Expose Enable Port Im	
Output Clock 2 Enabled A Warnings Info	⊥\ Symbol
Help •	OK Cance

Figure 3: PF_CCC_2_0 Output Clocks

3.3.1.2 IP Core PF_INIT_MONITOR_0



Figure 4: PF_INIT_Monitor_0 Bank Monitor

olarFire Initialization Monitor Conf	igurator
icrosemi:SgCore:PF_INIT_MONITOR:2.0.105	
Simulation Options	
FABRIC_POR_N assertion delay (ns)	
PCIE_INIT_DONE assertion delay (ns) 4	
USRAM_INIT_DONE assertion delay (ns) 5	PF INIT MONITOR 0
SRAM_INIT_DONE assertion delay (ns) 6	
DEVICE_INIT_DONE assertion delay (ns) 7	
Calibration monitor	PCIE_INIT_DONE
BANK_0_CALIB_STATUS assertion delay (ns)	USRAM_INIT_DONE -
BANK_1_CALIB_STATUS assertion delay (ns)	SRAM_INIT_DONE
BANK 2 CALTR STATUS assertion delay (ns)	DEVICE_INIT_DONE
	XCVR_INIT_DONE
BANK_4_CALIB_STATUS assertion delay (ns) 1	USRAM_INIT_FROM_SNVM_DONE -
BANK_5_CALIB_STATUS assertion delay (ns) 1	USRAM_INIT_FROM_UPROM_DONE
BANK_6_CALIB_STATUS assertion delay (ns) 1	USRAM_INIT_FROM_SPI_DONE
BANK_7_CALIB_STATUS assertion delay (ns)	SRAM INIT FROM SNVM DONE
3 VDDI monitor	SRAM INIT FROM UPROM DONE
BANK_0_VDDI_STATUS assertion delay (ns) 1	SRAM INIT FROM SPI DONE
BANK_1_VDDI_STATUS assertion delay (ns)	
BANK_2_VDDI_STATUS assertion delay (ns) 1	
BANK_4_VDDI_STATUS assertion delay (ns)	PF_INIT_MONITOR
BANK_5_VDDI_STATUS assertion delay (ns) 1	
BANK_6_VDDI_STATUS assertion delay (ns)	
BANK_7_VDDI_STATUS assertion delay (ns)	

Figure 5: PF_INIT_Monitor_0 Simulation Options

3.3.1.3 IP Core APB_WRAPPER_0

Configurator		_		\times
Configurator				
User:Private:APB_WRAPPER:	1.0			
Configuration				
APB_DWIDTH:	32		_	
APB_AWIDTH:	32		_	
- B C SAT CONSTANT WIDTH:	8		_	
			_	
	10		_	
g_3ii4_003_0wi0111.	110			
Help		ОК	Can	cel

Figure 6: APB_WRAPPER_0 Configuration

3.3.1.4 IP Core DDR_Memory_Arbiter_IP0_0

Configurator	- 🗆 ×	<
SF2 DDR Memory Arbit	er Configurator	
Microsemi:SolutionCore:ddr_memory_arb	iter:2.0.0	
Configuration	<u>-</u>	4
g_AXI_AWIDTH:	32	
g_AXI_DWIDTH:	64	
g_RD_CHANNEL1_AXI_BUFF_AWIDTH:	13	
g_RD_CHANNEL2_AXI_BUFF_AWIDTH:	13	
g_RD_CHANNEL3_AXI_BUFF_AWIDTH:	13	
g_RD_CHANNEL4_AXI_BUFF_AWIDTH:	13	
g_WR_CHANNEL1_AXI_BUFF_AWIDTH:	13	
g_WR_CHANNEL2_AXI_BUFF_AWIDTH:	13	
g_RD_CHANNEL1_HORIZONTAL_RESOLUTION;	1280	
g_RD_CHANNEL2_HORIZONTAL_RESOLUTION:	1280	
g_RD_CHANNEL3_HORIZONTAL_RESOLUTION:	1280	
a RD CHANNEL4 HORIZONTAL RESOLUTION:	1280	
	1280	
	1280	
	24	
g_RD_CHANNEL2_VIDEO_DATA_WIDTH:	24	
g_RD_CHANNEL3_VIDEO_DATA_WIDTH:	32	
g_RD_CHANNEL4_VIDEO_DATA_WIDTH:	8	
g_WR_CHANNEL1_VIDEO_DATA_WIDTH:	32	
g_WR_CHANNEL2_VIDEO_DATA_WIDTH:	32	
g_RD_CHANNEL1_BUFFER_LINE_STORAGE:	2	
q RD CHANNEL2 BUFFER LINE STORAGE:		

Figure 7: DDR_Memory_Arbiter_IP0 Configuration

Configurator	-		×
SF2 DDR Memory Arbi	ter Configu	irato	r
Microsemi:SolutionCore:ddr_memory_arb	iter:2.0.0		
g_WR_CHANNEL1_AXI_BUFF_AWIDTH:	13	_	
g_WR_CHANNEL2_AXI_BUFF_AWIDTH:	13	_	
g_RD_CHANNEL1_HORIZONTAL_RESOLUTION:	1280	-	
g_RD_CHANNEL2_HORIZONTAL_RESOLUTION:	1280	-	
g_RD_CHANNEL3_HORIZONTAL_RESOLUTION:	1280		
g_RD_CHANNEL4_HORIZONTAL_RESOLUTION:	1280		
g_WR_CHANNEL1_HORIZONTAL_RESOLUTION:	1280	_	
g_WR_CHANNEL2_HORIZONTAL_RESOLUTION:	1280	_	
g_RD_CHANNEL1_VIDEO_DATA_WIDTH:	24	_	
g_RD_CHANNEL2_VIDEO_DATA_WIDTH:	24	_	
g_RD_CHANNEL3_VIDEO_DATA_WIDTH:	32	_	
g_RD_CHANNEL4_VIDEO_DATA_WIDTH:	8	_	
g_WR_CHANNEL1_VIDEO_DATA_WIDTH:	32	_	
g_WR_CHANNEL2_VIDEO_DATA_WIDTH:	32	_	
g_RD_CHANNEL1_BUFFER_LINE_STORAGE:	2	_	
g_RD_CHANNEL2_BUFFER_LINE_STORAGE:	1	-	
g_RD_CHANNEL3_BUFFER_LINE_STORAGE:	1	-	
g_RD_CHANNEL4_BUFFER_LINE_STORAGE:	2	_	
g_WR_CHANNEL1_BUFFER_LINE_STORAGE:	1	-	
g_WR_CHANNEL2_BUFFER_LINE_STORAGE:	1		
testbench:	None	·	
License:	Obfuscated		-
Help 🔻	ОК	Cano	e

Figure 8: DDR_Memory_Arbiter_IP0 Configuration cont. ...

3.3.1.5 IP Core CoreAXI4Interconnect_0

rosenii.Direcceore.c	OREAXI4IN	TERCONNEC	T:2.4.102					
Core Configuration	Master Co	onfiguration	Slave	Configuration				
us Configuration			· ·	· ·				
Number of Masters:	1	•	Number of	Slaves: 1	•			
ID Width:	4	•	Data Width	n: 64	•			
Address Width:	32		User Width	: 1				
)ther Configuration —								
Number of Threads:		1	•	Max Outstanding 1	Transactions: 2	. <u> </u>	[
Upper Compare Bit:		31		Lower Compare Bit	: 1	2		
Slave FIFO Address	Depth:	4		Slave FIFO Data D	epth: 4	ł		
DWC Address FIFO I	Depth Ceiling	10		Crossbar Mode:		ī		

Figure 9: CoreAXI4Interconnect_0 Core Configuration

Configurator			×
CoreAXI4Interconnect Configurator			
Microsemi:DirectCore:COREAXI4INTERCONNECT:2.4.102			
Core Configuration Master Configuration Slave Configuration			-
Master0 Configuration			┐┝┛
M0 Type: AXI3 M0 Data Width: 64			
M0 DWC Data FIFO Depth: 16 🔹 M0 Register Slice: 🔽			
M0 Clock Domain Crossing:			
Master 1 Configuration			
M1 Type: AXI3 <u>v</u> M1 Data Width: 32 <u>v</u>			
M1 DWC Data FIFO Depth: 16 M1 Register Slice: 🔽			
M1 Clock Domain Crossing:			
Master2 Configuration			
M2 Type: AXI4 <u>v</u> M2 Data Width: 32 <u>v</u>			
M2 DWC Data FIEO Depthy 16 V M2 Depicter Slices V			
Help	ОК	Can	cel

Figure 10: CoreAXI4Interconnect_0 Master Configuration

Configurator	_		×
CoreAXI4Interconnect Configurator			
Microsemi:DirectCore:COREAXI4INTERCONNECT:2.4.102			
Core Configuration Master Configuration Slave Configuration			
Slave0 Configuration			
S0 Type: AXI3 S0 Data Width: 64			
S0 DWC Data FIFO Depth: 32 S0 Register Slice:			
S0 Clock Domain Crossing: 🗌 S0 Slot Base Vector 0			
S0 Slot Min Vector: 0x0 S0 Slot Max Vector: 0xffffff			
- Slave1 Configuration			
S1 Type: AXI4 S1 Data Width: 32 💌			
S1 DWC Data FIFO Depth: 16 S1 Register Slice:			
S1 Clock Domain Crossing: S1 Slot Base Vector: 1			
S1 Slot Min Vector: 0x0 S1 Slot Max Vector: 0xfffffff			
Help •	ОК	Can	el

Figure 11: CoreAXI4Interconnect_0 Slave Configuration

3.3.1.6 IP Core Display_Cntrll_0

Configurator	-		×
Display Controller	Configura	tor	
Microsemi:SolutionCore:display_co	ntroller:2.0.0		
Configuration			
g_DDR_AXI_AWIDTH:	32		
g_INPUT_X_W_RES_WIDTH:	12	_	
g_INPUT_Y_H_RES_WIDTH:	12	_	
g_VIDEO_FIFO_AWIDTH:	13	_	
g_INPUT_VIDEO_DATA_BIT_WIDTH:	24	_	
g_DEPTH_OF_VIDEO_PIXEL_FROM_DDR	: 1		
g_HORZ_SYNC_PULSE_POLARITY:	1		
g_VERT_SYNC_PULSE_POLARITY:	1		
g_INITIAL_LINES_TO_BUFFER:	6	_	
g_SUBSEQUENT_LINES_TO_BUFFER:	1	_	
g_HALF_EMPTY_THRESHOLD:	3840	_	
testbench:	User	•	
License:	Obfuscated		
Help -	ОК	Can	cel

Figure 12: Display_Cntrll_0 Configuration

3.3.1.7 IP Core DisplayEnhancement_0_0

Configurator	_	
Image Enhance	ment Confi	gurator
Microsemi:SolutionCore:Displ	ayEnhancements:2.0	0.0
Configuration		
g_YCbCr_DATA_BIT_WIDTH:	8	
g_B_C_SAT_CONSTANT_WIDTH:	8	
g_HUE_CONSTANT_WIDTH:	9	
g_SIN_COS_DWIDTH:	10	
g_SIN_COS_MEM_DEPTH:	180	
testbench:	User	
License:	Obfuscated	
Help 🔻	ОК	Cancel

Figure 13: DisplayEnhancement_0_0 Configuration

3.3.1.8 IP Core PF_CCC_3_0

Configurator		-	- 🗆	×
Clock Conditioning Circuitry (CCC)				
Microsemi:SgCore:PF_CCC:2.2.100				
Coofice ration DU-Single	1			
Clock Options PLL Output Clocks	1			
Input Frequency				
Input Frequency 166.666 MHz Backup Clock Bandwidth High = 0.073 MHz				
Delay Line				
Enable Delay Line				
🕫 Reference Clock Delay 🥤 Feedback Clock Delay				
Delay Steps: 1 📩				
		PF_CCC		
Power / Jitter				
Maximize VCO for Lowest Jitter VCO = 4752 MHz				
C Minimize VCO for Lowest Power				
E Feedback Mode				
Post-VCO 🔽				
E Features				
Integer Mode				
SSCG Modulation Finable Dunamic Reconfiguration Interface (DPI)				
Expose PowerDown Port	-	Symbol /		
Log				
Errors 🛦 Warnings 🕕 Info				
			-	
Help T		OK	Ca	ncel

Figure 14: PF_CCC_3_0 Clock Options PLL

Configurator		-		×
Clock Conditioning Circuitry (CCC)				
Microsemi:SgCore:PF_CCC:2.2.100				
Configuration PLL-Single				
Clock Options PLL Output Clocks				
For best results, put the highest frequency first.				
Output Clock 0				
₩ Enabled				
Requested Frequency 74.25 MHz C Actual Lower 74.25 MHz C Actual Higher 74.25 MHz Requested Phase 0 Degrees C Actual Lower 0 Degrees C Actual Lower 0 Degrees C Actual Higher 0 Degrees		PF_CCC_0	9	
Dynamic Phase Shifting Expose Enable Port Enable Bypass REF_PREDIV Global Clock Global Clock (Gated) HS I/O Clock Dedicated Clock				
Output Clock 1				
Enabled				
	- IV	Symbol /		
Log		<u>Symbol</u>		
🔳 Messages 🔞 Errors 🗼 Warnings 🌗 Info				
				_
Help •		ОК	Cance	e

Figure 15: PF_CCC_3_0 Output Clock

3.3.1.9 IP Core PF_DDR_CNTRLR_0_0

Configurator			_	
PolarEiro DDP2				
Microsemi:SystemBuilder:PF_DDR3:2.4.111				
	General Memory Initialization	Memory Timing	Controller	Misc.
PF_DDR3_UI_default_configuration	🗆 Тор			
Microsemi PolarFire Evaluation Kits PolarFire Evaluation Kit	Protocol DDR3 -			
MT41K1G8SN-125	Generate PHY only			
	Clock			
	Memory Clock Frequency (MHz)	666.666		
	CCC PLL Clock Multiplier	4	3	
	CCC PLL Reference Clock Frequen	cy (MHz) 166.667	-	
	User Logic Clock Rate	QUAD	Ē	
	User Clock Frequency	166.6665	-	
	Topology			
	Memory Format			
	DQ Width	16 💌		
	SDRAM Number of Ranks	1 .		
	Enable address mirroring on odd ra	anks 🗖		
	DQ/DQS group size	8 🔻		
Apply New preset	Row Address width	16		
	Column Address Width	10		
	Rank Address Width	2		
	Bank Address Width]3		
	Enable DM	JDM 💌		
	Enable Parity/Alert			
	Enable ECC	Г		
	Number of clock outputs	1 💌		-
			1	
Help			OK	Cancel

Figure 16: PF_DDR_CNTRLR_0_0 General

Configurator	- 0	×
PolarFire DDR3		
Microsemi:SystemBuilder:PF_DDR3:2.4.111		
	General Memory Initialization Memory Timing Controller Misc.	_ _
PF_DDR3_UI_default_configuration	Mode Register 0	
Microsemi PolarFire Evaluation Kits PolarFire Evaluation Kit	Read Burst Type Sequential	
MT41K1G8SN-125	Burst Length Fixed BL8	
	Memory CAS Latency 9	
	Mode Register 1	
	ODT Rtt Nominal Value ODT Disabled	
	Memory Additive CAS Latency Disabled	
	Output Drive Strength RZQ/6	\vdash
Apply New preset	Mode Register 2	
	Self Refresh Temperature Normal	
	Memory Write CAS Latency 7	
	Partial Array Self Refresh Full	
	Dynamic ODT (Rtt_WR) Dynamic ODT off	Ŀ
Help 🔻	ОК Са	ancel

Figure 17: PF_DDR_CNTRLR_0_0 Memory Initialization

Configurator			_		×
Delar Eiro DDD2					
Microsemi:SystemBuilder:PF DDR3:2.4.111					
	General Memory Initialization	Memory Timing	Controller	Misc.	
PF_DDR3_UI_default_configuration	□ Timing parameters dependent o	n speed bin			
Microsemi PolarFire Evaluation Kits PolarFire Evaluation Kit	tRAS (ns) 36				
□- MPF300T MT41K1G8SN-125	tRCD (ns) 13.5				
	tRP (ns) 13.5				
	tRC (ns) 49.5				
	tWR (ns) 15				
	HEALW () 20				
	Timing parameters dependent of	n speed bin and clock	frequency		
	tWTR (cycles) 5	-	,		
	tRRD (ns)	-			
	4070 (cs) 7.5	-			
	Timing parameters dependent of	n operating condition			
	tREFI (us) 7.8	n operating condition			
	Timing parameters dependent of	n speed bin and page	e size		
	tRFC (ns) 350				
Apply New preset	□ Other Timing parameters				
	tZQinit (cycles)	512			
	ZQ Calibration Type	Short 💌			
	tZQCS (cydes)	64			
	tZQoper (cycles)	256			
	Enable User ZQ Calibration Controls				
	Automatic ZQ Calibration Period (us)	200			
					-
Holp Y			OK	1	col
nep			UK		lei

Figure 18: PF_DDR_CNTRLR_0_0 Memory Timing

Configurator		— 🗆 X
PolarFire DDR3		
Microsemi:SystemBuilder:PF_DDR3:2.4.111		
	General Memory Initialization Memory Timing C	ontroller Misc.
PF_DDR3_UI_default_configuration JEDEC Microsemi PolarFire Evaluation Kits PolarFire Evaluation Kit	Instance Select	
→ MPF300T → MT41K1G8SN-125	User Interface	
	Fabric Interface AXI3	
	AXI Width 64	
	AXI ID Width 4	
	Efficiency	
	Enable Activate/Precharge look-ahead	
	Command queue depth 3	
	Enable User Refresh Controls	
	Address Ordering Chip-Row-Bank-Col 💌	
	Misc	
Apply New preset	Enable RE-INIT Controls	
	ODT Activation Settings on Write	
	Enable Rank0 - ODT0 🔽 Enable Rank0 - ODT1 🔽	
	Enable Rank1 - ODT0 🔽 Enable Rank1 - ODT1 🔽	
	ODT Activation Settings on Read	
	Enable Rank0 - ODT0 🗌 Enable Rank0 - ODT1 🗖	
	Enable Rank1 - ODT0 🗆 Enable Rank1 - ODT1 🗖	
		•
Help 🔻		OK Cancel

Figure 19: PF_DDR_CNTRLR_0_0 Controller

User Guide

O Configurator	-		×
PolarFire DDR3 Microsemi:SystemBuilder:PF_DDR3:2.4.111			
	General Memory Initialization Memory Timing Controller	Misc.	1
PF_DDR3_UI_default_configuration JEDEC Microsemi PolarFire Evaluation Kits PolarFire Evaluation Kit	 Simulation Options Simulation Mode Fast (skip training and settling time) Throughput Options Pipe Lining 		
Apply New preset			.
Help 🔻	ОК	Car	ncel

Figure 20: PF_DDR_CNTRLR_0_0 Misc.

3.3.2 Smart Design cam_ar0331_mipi



3.3.2.1 IP Core MIPI_RX_IOD_0

PolarFire IOD Generic Receive Interfaces							
Microsemi:SystemBuilder:PF_IOD_GENERIC_RX:2.0.123							
	Configuration Advanced						
PF_IOD_GENERIC_RX_UI_default_configuration	□ I/O						
DDR - aligned clock and data							
DDR - centered clock and data	Data rate	800 Mbps					
DDRX - centered clock and data		1					
DDRX - aligned clock and data							
DDRX - fractional aligned clock and data	Number of data I/Os	4					
DDRX - fractional dynamic data alignment							
E DDRX - dynamic data alignment	Clock to data relationship	Dunamic					
RX_DDRX_B_G_DYN_X2	Clock to data relationship	joynamic					
RX_DDRX_B_G_DVN_X3.5		_					
	Differential clock input	V					
	Differential data inputs						
	MIDI low power escape suppor	et 🔽					
	MIPI low power escape suppor						
	Input clock ratio	Same as fabric clock ratio					
	E Fabric						
	Fabric clock ratio	•					
	Data deserialization ratio 8						
	Fabric clock source	pric global clock					
	Enable BITSLIP port						
1							

Figure 21: MIPI_RX_IOD_0 Configuration

PolarFire IOD Generic Rec	eive Interfaces
Microsemi:SystemBuilder:PF_IOD_GENERIC_RX:2	.0.123
	Configuration Advanced
PF_IOD_GENERIC_RX_UI_default_configuration DDR - aligned clock and data	Fabric topology
DDR - centered clock and data DDRX - centered clock and data DDRX - aligned clock and data	Fabric global dock from external source
DDRX - fractional aligned clock and data DDRX - fractional dynamic data alignment	Received data organization Received data independent per inputs
RX_DDRX_B_G_DYN_X2 RX_DDRX_B_G_DYN_X2 RX_DDRX_B_G_DYN_X3.5	RXD bus width 4
RX_DDRX_B_G_DYN_X4	RXCTL bus width
- RX_DDRX_B_R_DYN_X3.5 - RX_DDRX_B_R_DYN_X4	Expose RX raw data
RX_DDRX_B_R_DYN_X5	Expose fractional dock parallel data
	Timing
	Expose dynamic delay control
	Add delay line on clock for RX_DDR_G_A/C
	Clock delay line tap 0
	Expose extra training control ports
	□ 1/0
	Enable RX_CLK_ODT_EN for LVDS failsafe
	Enable RXD_ODT_EN for LVDS failsafe

Figure 22: MIPI_RX_IOD_0 Advanced

Current configuration
Interface: RX_DDRX_B_G_DYN
Max data rate per I/O: 1600 Mbps Current data rate per I/O: 800 Mbps Total data rate: 3200.00 Mbps Maximum number of data I/O: one bank
I/O Capture Clock: High Speed I/O clock (HS_IO_CLK) I/O clock speed: 400.00 MHz Fabric clock speed: 100.00 MHz
Imming: Q RX_CLK Q <t< td=""></t<>
.eg RX_CLK_G ** // .eg L0_RX_DATA[7:0] * //
* Waveform post bit-slip ** See user guide for actual latency between I/O and Fabric

Figure 23: MIPI_RX_IOD_0 Current configuration

Receiver interface								
Name	Ratio	Clock to data relationship	I/O clock	Fabric clock	Max data rate	Lane organization	One lane max	Dynamic bit training
RX_DDR_G_A	1	Aligned	Global	Global	690	×	×	×
RX_DDR_R_A	1	Aligned	Regional	Regional	500	~	v	×
RX_DDR_G_C	1	Centered	Global	Global	690	×	×	×
RX_DDR_R_C	1	Centered	Regional	Regional	500	V	v	×
RX_DDRX_B_G_A	2, 3.5, 4, 5	Aligned	High Speed I/O Clock	Global	700	~	×	×
RX_DDRX_B_R_A	2, 3.5, 4, 5	Aligned	High Speed I/O Clock	Regional	500	~	~	×
RX_DDRX_B_G_C	2, 3.5, 4, 5	Centered	High Speed I/O Clock	Global	700	V	×	×
RX_DDRX_B_R_C	2, 3.5, 4, 5	Centered	High Speed I/O Clock	Regional	500	V	~	×
RX_DDRX_B_G_FA	2, 3.5, 4, 5	Fractional Aligned	High Speed I/O Clock	Global	700	~	×	×
RX_DDRX_B_G_DYN	2, 3.5, 4, 5	Dynamic	High Speed I/O Clock	Global	1000, 1600, 1600, 1600	v	×	v
RX_DDRX_B_R_DYN	2, 3.5, 4, 5	Dynamic	High Speed I/O Clock	Regional	500	~	v	v

Figure 24: MIPI_RX_IOD_0 Receiver interface

User Guide

3.3.2.2 IP Core PF_CCC_0

Configurator			-		×
Clock Conditioning Circuitry (CCC)					
Microsemi:SgCore:PF CCC:2.2.100					
Configuration PLL-Single					
Clock Options PLL Output Clocks					
Input Frequency					
Input Frequency 19.5 MHz 🗌 Backup Clock					
Bandwidth High = 0.348 MHz					
Delay Line					
Enable Delay Line					
🕫 Reference Clock Delay 🥤 Feedback Clock Delay					
Delay Steps: 1					
		PF.	_CCC_0		
Power / Jitter		REF_CLK_0	OUT1_FAE PLL_U	00K_0 -	
Maximize VCO for Lowest Jitter VCO = 4992 MHz		P	PF_CCC	_	
C Minimize VCO for Lowest Power					
Feedback Mode					
Post-VCO 💌					
E Features					
Tinteger Mode					
SSCG Modulation					
Enable Dynamic Reconfiguration Interface (DRI)					
Expose PowerDown Port					
					_
	<u> </u>	Symbol /			
🔳 Messages 👹 Errors 🔥 Warnings 🕕 Info					
нер 🔻			ОК	Can	cel

Figure 25: PF_CCC_0 Clock Options PLL

onfigurator			
<pre>modentSqCoreF_CCC22100 Configuration FLL Grige Configuration FLL</pre>	lock Conditioning Circuitry (CCC)		
Configuration PLL Sould Test and the hybrid frequency first. Configuration PLL Output Clocks Vester reading, but the hybrid frequency first. Vester reading frequency f	crosemi:SgCore:PF_CCC:2.2.100		
the deplote RL Output Oods The transfer all the highest frequency fort. • Charlet Clock The Requested Frequency 51.5 Mits Actual Lower 33.5 Mits Actual Higher 33.5 Mits Requested Frequency 51.5 Mits Actual Lower 33.5 Mits Actual Higher 35.5 Mits Requested Frequency 51.5 Mits Actual Lower 30.5 Mits Actual Higher 35.5 Mits Requested Frequency 51.5 Mits Actual Lower 30.5 Mits Actual Higher 37.5 Mits Pointer Clock (Galeed) HIS 17.0 Clock Dedicated Clock • Charlet Clock HIME Clock (Galeed) HIS 17.0 Clock Dedicated Clock • Charlet Clock HIME Clock HIME Clock HIME Dedicated Clock • Charlet Clock HIME Clock HIME Clock HIME Dedicated Clock • Charlet Frequency Mits Actual Lower Mits Actual Higher Mits • Charlet Frequency Mits Actual Lower Mits Actual Higher Degrees • Charlet Frequency Mits Actual Lower Mits Actual Higher Mits • Charlet Frequency Mits Actual Higher Degrees Return HIME HIME HIME Degrees Return HIME HIME HIME Degrees Return HIME HIME HIME HIME HIME HIME HIME HIME	Configuration PLL-Single	^	
ret reade, put the highest frequency first. • orpand Cock • Requested frequency [155] • Orpand Cock • Orpand Cock • Orpand Cock • Orpand Cock <td>Clock Options PLL Output Clocks</td> <td></td> <td></td>	Clock Options PLL Output Clocks		
Output Clock 0 © Output Clock 0 Requested Frequency [15.5] Mriz C Actual Higher 19.5 Mriz C Actual Higher 0 Degrees C Actual	For best results, put the highest frequency first.		
<pre>w to w to</pre>	Output Clock 0		
Requested Frequency 19.5 Mtz Actual Lower 19.5 Mtz Actual Higher 19.5 Mtz Propress Actual Lower Degrees Actual Higher 19.5 Mtz Global Clock Global Clock Global Clock Degrees Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Global Clock Global Clock Global Clock Clock Propress Actual Lower 78 Mtz Actual Higher 78 Mtz Propress Octool Degrees Actual Lower 78 Mtz Propress Octool Clock Degrees Actual Higher 78 <	I⊄ Enabled		
Image: Section of the second of the second of the section of the section of the	Requested Frequency 19.5 MHz C Actual Lower 19.5 MHz C Actual Higher 19.5 MHz Requested Phase 0 Degrees C Actual Lower 0 Degrees C Actual Higher 0 Degrees		
	Dynamic Phase Shifting Expose Enable Port Enable Bypass REF_PREDIV		
Output Clock 1 Preobled Requested Frequency 78 MHz Actual Lower 78 MHz Actual Higher 78 MHz Requested Phase 0 Degrees Actual Lower 0 Degrees Actual Higher 0 Degrees Oynamic Phase Shifting Expose Enable Port Enable Bypass REF_REDIV Global Clock (Gated) THS 1/0 Clock Output Clock 2 Requested Frequency 100 MHz Actual Lower MHz Actual Higher MHz Requested Frequency 100 MHz Actual Lower Degrees Actual Higher Degrees Output Clock 2 Domanic Phase Shifting Expose Enable Port Enable Bypass REF_REDIV wessages S Errors Actual Lower The Enable Bypass REF_REDIV wessages S Errors Actual Lower The Enable Bypass REF_REDIV wessages Actual Higher MHz Messages Actual Higher Actual Higher MHz Messages Actual Higher Actual Higher MHz Messages Actual Higher Actual Lower Actual Higher MHz Messages Actual Higher Actual Lower Actual Higher MHz Messages Actual Higher Actual Lower Actual Higher Actual Actual Higher Actual Actual Higher Actual Actual Higher Actual Higher Actual Actual Higher Actual Actual Higher Actual Higher Actual	Global Clock Gated) HS I/O Clock Dedicated Clock		PE CCC 0
Image: Shifting Expose Enable Port Image: Enabled Image: Shifting Expose Enable Port Image: Enabled Image: Enabled Image: Enable Image: Enable <	Output Clock 1		OUTD_FABCLK_0
Requested Frequency 73 MHz Actual Lower 73 MHz Actual Higher 73 MHz Requested Phase 0 Degrees Actual Lower 0 Degrees Actual Higher 0 Degrees I Ontput Clock 2 I Enable Requested Prequency 100 MHz Actual Lower MHz Actual Higher MHz I Requested Frequency 100 MHz Actual Lower MHz Actual Higher MHz Requested Frequency 100 MHz Actual Lower MHz Actual Higher MHz Requested Prequency 100 MHz Actual Lower MHz Actual Higher MHz Requested Prequency 100 MHz Actual Lower MHz Actual Higher MHz Requested Prequency 100 MHz Actual Lower MHz CActual Higher MHz Requested Prequency 100 MHz Actual Lower MHz Degrees Vnamic Phase Shiftino Excose Enable Port Enable Byoass REF PREDIV Image: Smbd	I Frabled		PF_CCC
Image: Provide Phase Shifting Expose Enable Port Enable Bypass REF_PREDIV Image: Global Clock Global Clock (Gated) HS I/O Clock Dedicated Clock Image: Clock 2 I	Requested Frequency 78 MHz C Actual Lower 78 MHz C Actual Higher 78 MHz Requested Phase 0 Degrees C Actual Lower 0 Degrees C Actual Higher 0 Degrees		
Image: State of the second	Dynamic Phase Shifting Expose Enable Port Enable Bypass REF_PREDIV		
	✓ Global Clock □ Global Clock (Gated) □ HS I/O Clock □ Dedicated Clock		
Enabled			
Requested Frequency 100 MHz C Actual Lower MHz C Actual Higher MHz Requested Phase 0 Degrees C Actual Lower Degrees C Actual Higher Degrees Dvnamic Phase Shifting E Exoose Enable Port E Enable Bvoass REF PREDIV V V Messages Serrors Warnings Image:			
Requested Frequency 100 MHz C Actual Lower MHz C Actual Lower MHz C Actual Higher MHz Requested Phase 0 Degrees C Actual Lower Degrees C Actual Higher Degrees Info Info Messages Info Info OK Cancel			
Requested Phase 0 Degrees C Actual Lower Degrees C Actual Higher Degrees Image: Dvnamic Phase Shifting Image: Excose Enable Port Image: Enable Bvpass Imag	Requested Frequency 100 MHz C Actual Lower MHz C Actual Higher MHz		
	Requested Phase 0 Degrees C Actual Lower Degrees C Actual Higher Degrees		
Messages 😵 Errors 🔺 Warnings 🌒 Info	□ Dvnamic Phase Shifting □ Expose Enable Port □ Enable Bvpass	· •	Symbol
telp *	🗄 Messages 😵 Errors 🔺 Warnings 🌐 Info		
telp 🖌			
telp 🔹			
	ielp 🔹		OK Cance

Figure 26: PF_CCC_0 Output Clocks

3.3.2.3 IP Core MIPI_CSI2_RX_PF_IP0_0

Configurator			-		×
MIPI CSI2	RxDecoder	PF	Config	urato	or
Microsemi:SolutionCo	re:mipicsi2rxdecode	rPF:2.3	2.5		
Configuration					1
g_DATAWIDTH:	8				
g_LANE_WIDTH:	4				
g_NUM_OF_PIXELS:	1				
g_INPUT_DATA_INVERT	: 0 💌				
g_BUFF_DEPTH:	1280				
License:	Obfuscated				
Help 🔹		[ОК	Cano	:el

Figure 27: MIPI_CSI2_RX_PF_IP0_0 Configuration

3.3.3 Smart Design PROC_SUBSYSTEM

3.3.3.1 IP Core Mi_V_Processor_0_0



Figure 28: RV32IMA_L1_AHB Configuration

3.3.3.2 IP Core COREJTAGDEBUG_0

Configurator	-		×
CoreJTAGDebug Configurator			
Microsemi:DirectCore:COREJTAGDEBUG:3.1.100			
Configuration			_
General Configuration			
Number of Debug Targets 1			
UJTAG_BYPASS			
Debug_Target_0			
Target 0 IR Code 0x55 Active-high target reset Targ	et 0 🔽		
Debug_Target_1			
Target 1 IR Code 0x56 Active-high target reset Targ	et 1 🔽		
Debug_Target_2			
Target 2 IR Code 0x57 Active-high target reset Targ	et 2 🔽		
Debug_Target_3			
Help •	— ОК	Can	

Figure 29: CoreJTAGDebug Configuration

3.3.3.3 IP Core CoreAHBLite_1_0

Configurator							-		×
CoreAHBLite Confi	gurato	r							
Microsemi:DirectCore:CoreAHBLite	:5.4.102								
Configuration Interface Cont	figuration								-
Memory space									
Memory space:		16	6 64KB slots, plus reserv	ved space, plus 1 huge (2GB) sl	lot beginning at add	ress 0x80000000 💌			
Address range seen by slave con	nected to huge	e (2GB) slot interface: 🔿	0x00000000 - 0x7FFFf	FFFF © 0x80000	0000 - 0xFFFFFFFF				
Allocate memory space to combined re	egion slave								
Slot 0: 🔽 Slot 1: 🗖	Slot 2: 🗖	Slot 3:							
Slot 4: 🗂 Slot 5: 🗂	Slot 6: 🗖	Slot 7:							
Slot 8: 🗂 Slot 9: 🗂	Slot 10: Г	Slot 11:							
Slot 12: 🔽 Slot 13: 🗖	Slot 14: Г	Slot 15: Г							
Enable Master access									
M0 can access slot 0:	Γ	M1 can access slot 0:	Π	M2 can access slot 0:	Γ	M3 can access slot 0:			
M0 can access slot 1:		M1 can access slot 1:		M2 can access slot 1:		M3 can access slot 1:			
M0 can access slot 2:	Γ	M1 can access slot 2:		M2 can access slot 2:		M3 can access slot 2:			
M0 can access slot 3:		M1 can access slot 3:		M2 can access slot 3:		M3 can access slot 3:			
M0 can access slot 4:		M1 can access slot 4:		M2 can access slot 4:		M3 can access slot 4:			
M0 can access slot 5:		M1 can access slot 5:		M2 can access slot 5:		M3 can access slot 5:			
M0 can access slot 6:		M1 can access slot 6:		M2 can access slot 6:		M3 can access slot 6:			
M0 can access slot 7:		M1 can access slot 7:		M2 can access slot 7:		M3 can access slot 7:			
M0 can access slot 8:		M1 can access slot 8:		M2 can access slot 8:		M3 can access slot 8:			
M0 can access slot 9:		M1 can access slot 9:	Г	M2 can access slot 9:		M3 can access slot 9:			
M0 can access slot 10:	Г	M1 can access slot 10:		M2 can access slot 10:		M3 can access slot 10:			
M0 can access slot 11:	Г	M1 can access slot 11:	Г	M2 can access slot 11:	Г	M3 can access slot 11:	Г		
M0 can access slot 12:		M1 can access slot 12	-	M2 can access slot 12:		M3 can access plot 12:			
NU Carl access SIUL 12:		mi can access si0t 12:	_	m2 can access slot 12:		no can access side 12:			-
Help -		M1 con accoss slot 12:		Million according to 12:		M2 can accord dat 19.	ОК	Cano	el

Figure 30:	CoreAHBLite	10	Configuration
		_'	•••inigal all off

reAHBI ite Conf	igurato)r						
osemi:DirectCore:CoreAHBLit	e:5.4.102							
M0 can access slot 2:		M1 can access slot 2:		M2 can access slot 2:		M3 can access slot 2:		
M0 can access slot 3:		M1 can access slot 3:		M2 can access slot 3:		M3 can access slot 3:		
M0 can access slot 4:		M1 can access slot 4:		M2 can access slot 4:		M3 can access slot 4:		
M0 can access slot 5:		M1 can access slot 5:		M2 can access slot 5:		M3 can access slot 5:		
M0 can access slot 6:		M1 can access slot 6:		M2 can access slot 6:		M3 can access slot 6:	Γ	
M0 can access slot 7:		M1 can access slot 7:		M2 can access slot 7:		M3 can access slot 7:		
M0 can access slot 8:		M1 can access slot 8:		M2 can access slot 8:		M3 can access slot 8:		
M0 can access slot 9:		M1 can access slot 9:		M2 can access slot 9:		M3 can access slot 9:		
M0 can access slot 10:		M1 can access slot 10:		M2 can access slot 10:		M3 can access slot 10:		
M0 can access slot 11:		M1 can access slot 11:		M2 can access slot 11:		M3 can access slot 11:		
M0 can access slot 12:		M1 can access slot 12:		M2 can access slot 12:		M3 can access slot 12:		
M0 can access slot 13:		M1 can access slot 13:		M2 can access slot 13:		M3 can access slot 13:		
M0 can access slot 14:		M1 can access slot 14:		M2 can access slot 14:		M3 can access slot 14:	Γ	
M0 can access slot 15:		M1 can access slot 15:		M2 can access slot 15:		M3 can access slot 15:		
M0 can access slot 16 (combined	d/huge): 🔽	M1 can access slot 16 (combine	d/huge): 🗖	M2 can access slot 16 (combined	l/huge): 🗖	M3 can access slot 16 (combine	ed/huge): 🗖	
ench: User 💌								

Figure 31: CoreAHBLite_1_0 Configuration cont. ...

User Guide

Configurator	-		×
CoreAHBLite Configurator			
Microsemi:DirectCore:CoreAHBLite:5.4.102			
Configuration Interface Configuration			-
□ Master Configuration			
Master0 Interface AHB Mirror Master BIF 💌 Master1 Interface AHB Mirror Master BIF 💌			
Master2 Interface AHB Mirror Master BIF 💌 Master3 Interface AHB Mirror Master BIF 💌			
□ Slave Configuration			
Slave0 interface 🛛 AHB Mirror Slave BIF 💌 Slave1 Interface 🖉 AHB Mirror Slave BIF 💌 Slave2 Interface 🖉 AHB Mirror Slave BIF 💌 Slave3 Interface 🖉 AHB Mirror Slave BIF 💌	ve BIF	·	
Slave4 Interface 🛛 AHB Mirror Slave BIF 💌 Slave5 Interface 🖉 AHB Mirror Slave BIF 💌 Slave6 Interface 🖾 AHB Mirror Slave BIF 💌 Slave7 Interface 🖾 AHB Mirror Slave BIF	ve BIF 👱	J	
Slave8 Interface 🛛 AHB Mirror Slave BIF 💌 Slave9 Interface 🖾 AHB Mirror Slave BIF 💌 Slave10 Interface 🖾 AHB Mirror Slave BIF 💌 Slave11 Interface 🖾 AHB Mirror Slave BIF	ve BIF 👱	·	
Slave 12 Interface 🛛 AHB Mirror Slave BIF 💌 Slave 13 Interface 🖾 HB Mirror Slave BIF 💌 Slave 14 Interface 🖾 HB Mirror Slave BIF 💌 Slave 15 Interface 🖾 HB Mirror Slave BIF	ve BIF 📘	·	
Slave 15 Interface AHB Mirror Slave BIF 💌			
			-
Help	ОК	Can	cel

Figure 32: CoreAHBLite_1_0 Interface Configuration

3.3.3.4 IP Core CoreAHBLite_0

Configurator							-		×
CoreAHBLite Conf	igurato	r							
Microsemi:DirectCore:CoreAHBLit	te:5.4.102								
Configuration Interface Con	nfiguration								-
Memory space									
Memory space:		4GB a	addressable space ap	oportioned into 16 slave slots, e	each of size 256MB	•			
Address range seen by slave co	nnected to huge	e (2GB) slot interface: C 0x	00000000 - 0x 7 FFFF	FFF © 0x80000	000 - 0xFFFFFFFF				
Allocate memory space to combined	region slave								
Slot 0: 🗆 Slot 1: 🗖	Slot 2:	Slot 3:							
Slot 4: 🗖 Slot 5: 🗖	Slot 6: 🕅	Slot 7:							
Slot 8: 🗖 Slot 9: 🗖	Slot 10: 🗆	Slot 11:							
Slot 12: 🗖 Slot 13: 🗖	Slot 14: 🗖	Slot 15:							
Enable Master access									
M0 can access slot 0:		M1 can access slot 0:		M2 can access slot 0:		M3 can access slot 0:			
M0 can access slot 1:		M1 can access slot 1:	Γ	M2 can access slot 1:		M3 can access slot 1:	Γ		
M0 can access slot 2:		M1 can access slot 2:		M2 can access slot 2:		M3 can access slot 2:			
M0 can access slot 3:		M1 can access slot 3:		M2 can access slot 3:		M3 can access slot 3:			
M0 can access slot 4:		M1 can access slot 4:		M2 can access slot 4:		M3 can access slot 4:			
M0 can access slot 5:		M1 can access slot 5:		M2 can access slot 5:		M3 can access slot 5:			
Help 🔻							ОК	Cano	cel

Figure 33: CoreAHBLite_0 Configuration

User Guide

Configurator							-		
oreAHBLite Conf	igurato	r							
icrosemi:DirectCore:CoreAHBLit	e:5.4.102								
M0 can access slot 3:		M1 can access slot 3:		M2 can access slot 3:		M3 can access slot 3:			
M0 can access slot 4:		M1 can access slot 4:		M2 can access slot 4:		M3 can access slot 4:			
M0 can access slot 5:		M1 can access slot 5:		M2 can access slot 5:		M3 can access slot 5:			
M0 can access slot 6:		M1 can access slot 6:		M2 can access slot 6:		M3 can access slot 6:			
M0 can access slot 7:	~	M1 can access slot 7:		M2 can access slot 7:		M3 can access slot 7:			
M0 can access slot 8:		M1 can access slot 8:		M2 can access slot 8:		M3 can access slot 8:			
M0 can access slot 9:		M1 can access slot 9:		M2 can access slot 9:		M3 can access slot 9:			
M0 can access slot 10:		M1 can access slot 10:		M2 can access slot 10:		M3 can access slot 10:			
M0 can access slot 11:		M1 can access slot 11:		M2 can access slot 11:		M3 can access slot 11:			
M0 can access slot 12:		M1 can access slot 12:		M2 can access slot 12:		M3 can access slot 12:			
M0 can access slot 13:		M1 can access slot 13:		M2 can access slot 13:		M3 can access slot 13:			
M0 can access slot 14:		M1 can access slot 14:		M2 can access slot 14:		M3 can access slot 14:			
M0 can access slot 15:		M1 can access slot 15:		M2 can access slot 15:		M3 can access slot 15:			
M0 can access slot 16 (combined	d/huge): □	M1 can access slot 16 (combined/huge)): 🗖	M2 can access slot 16 (combined/huge	≥): □	M3 can access slot 16 (combined/hu	ge): Г		
stbench: User 💌									
Helo 🔸							OK	Can	

Figure 34: CoreAHBLite_0 Configuration cont. ...

Configurator –	□ ×
CoreAHBLite Configurator	
Microsemi:DirectCore:CoreAHBLite:5.4.102	
Configuration Interface Configuration	<u> </u>
Master Configuration	
Master0 Interface AHB Mirror Master BIF 💌 Master1 Interface AHB Mirror Master BIF 💌	
Master2 Interface AHB Mirror Master BIF 💌 Master3 Interface AHB Mirror Master BIF 💌	
□ Slave Configuration	- 11
Slave0 interface 🛛 AHB Mirror Slave BIF 💌 Slave1 Interface 🖾 AHB Mirror Slave BIF 💌 Slave2 Interface 🖾 AHB Mirror Slave BIF 💌 Slave3 Interface 🖾 AHB Mirror Slave BIF 💌	
Slave4 Interface AHB Mirror Slave BIF 💌 Slave5 Interface AHB Mirror Slave BIF 💌 Slave6 Interface AHB Mirror Slave BIF 💌	
Slave8 Interface 🛛 AHB Mirror Slave BIF 💌 Slave9 Interface 🔍 AHB Mirror Slave BIF 💌 Slave10 Interface 🖾 AHB Mirror Slave BIF 💌 Slave11 Interface 🖾 AHB Mirror Slave BIF 💌	
Slave 12 Interface AHB Mirror Slave BIF 💌 Slave 13 Interface AHB Mirror Slave BIF 💌 Slave 14 Interface AHB Mirror Slave BIF 💌 Slave 15 Interface AHB Mirror Slave BIF	μ
Slave 16 Interface AHB Mirror Slave BIF 💌	
Help •	Cancel

Figure 35: CoreAHBLite_0 Interface Configuration

3.3.3.5 IP Core CoreAPB3_0

CoreAPB3	Configu					
icrosemi:DirectC	-	rator				
Configuration	ore:CoreAPB3:4	1.1.100				
Data Width Configu	ration					 _
APB Master Da	ata Bus Width 🔎	32-bit C	16-bit	C 8-bit		
Address Configurat	ion					_
Number of add	lress bits driven b	y master:		16	•	
Position in slav	e address of upp	er 4 bits of maste	er address:	[27:24] (Ignored if master address width >= 32 bits)	•	
Indirect Addre	ssing:			Not in use	•	
Allocate memory sp	ace to combined i	region slave				
Slot 0: 🗖	Slot 1: 🗔	Slot 2:	Slot 3:			
Slot 4: 🗔	Slot 5:	Slot 6: 🗔	Slot 7:	Г		
Slot 8:	Slot 9:	Slot 10: 🕅	Slot 11:			
Slot 12: 🗖	Slot 13: 🕅	Slot 14: 🕅	Slot 15:	Γ		
Enabled APB Slave	Slots					
Slot 0: 🗖	Slot 1: 🔽	Slot 2: 🔽	Slot 3:	v		
Slot 4: 🔽	Slot 5: 🔽	Slot 6: 🔽	Slot 7:	v		
Slot 8: 🔽	Slot 9: 🔽	Slot 10: 🕅	Slot 11:			
Slot 12: 🕅	Slot 13: 🗖	Slot 14: 🗖	Slot 15:			

Figure 36: CoreAPB3_0 Configuration

3.3.3.6 IP Core CoreUARTapb_0

Configurator		_		×
CorellARTaph C	onfigu	rat	or	
Microsemi:DirectCore:CoreU/	RTapb:5.6.1	1 CI C		
Configuration				
Core Configuration				-1
TX FIFO: Dis	able TX FIFO	•		
RX FIFO: Dis	able RX FIFO	•		
Configuration: Pro	grammable	•		
Baud Value: 1				
Character Size: 7 b	its	Ŧ		
Parity: Par	ity Disabled	$\overline{\nabla}$		
RX Legacy Mode: Dis	abled	•		
FIFO Implementation: In	RAM	$\overline{\nabla}$		
Baud Value Precision				
Enable Extra Precision:				
Fractional Part of Baud Val	ue: +0.0	Ŧ		
Testbench: User 💌				
License: Obfuscated				
Help 🔻	ОК		Cance	

Figure 37: CoreUARTapb_0 Configuration

3.3.3.7 IP Core CoreGPIO_IN

Configurator	-		×
CoreGPIO Configurator			
Configuration Global Configuration APB Data Width: 32 Number of I/Os: 32 Single-bit interrupt port: Disabled Output enable: Internal			•
I/O bit 0 Output on Reset: Image: Street Config: I/O Type: Input Interrupt Type: Disabled	•		
I/O bit 1 Output on Reset: 0 - Fixed Config: V I/O Type: Input Interrupt Type: Disabled	•		
I/O bit 2 Output on Reset: 0 - Fixed Config: V I/O Type: Input Interrupt Type: Disabled	•		
I/O bit 3 Output on Reset: 0 V Fixed Config: V I/O Type: Input V Interrupt Type: Disabled	•		
I/O bit 4 Output on Reset: 0 V Fixed Config: V I/O Type: Input V Interrupt Type: Disabled	•		
I/O bit 5 Output on Reset: 0 - Fixed Config: 🗹 I/O Type: Input 💌 Interrupt Type: Disabled	•		
I/O bit 6 Output on Reset: 0 - Fixed Config: 🗸 I/O Type: Input - Interrupt Type: Disabled	•		•
нер •	к	Cancel	

Figure 38: CoreGPIO_IN Configuration (all IOs have the same configuration)

3.3.3.8 IP Core CoreGPIO_OUT

Configurator	-		×
CoreGPIO Configurator			
Microsemi:DirectCore:CoreGP10:3.2.102			
Configuration			-
Global Configuration			
APB Data Width: 32 Number of I/Os: 32			
Single-bit interrupt port: Disabled 💌 Output enable: Internal 💌			
_T/O bit 0			
Output on Reset: 0 💌 Fixed Config: 🔽 I/O Type: Output 💌 Interrupt Type: Disabled	•		
I/O bit 1			
Output on Reset: 0 💌 Fixed Config: 🗹 I/O Type: Output 💌 Interrupt Type: Disabled	•		
_I/O bit 2			
Output on Reset: 0 💌 Fixed Config: 🗹 I/O Type: Output 💌 Interrupt Type: Disabled	•		
_I/O bit 3			
Output on Reset: 0 💌 Fixed Config: 🗹 I/O Type: Output 💌 Interrupt Type: Disabled	•		
_T/O bit 4			
Output on Reset: 0 💌 Fixed Config: 🗹 I/O Type: Output 💌 Interrupt Type: Disabled	•		
I/O bit 5			
Output on Reset: 0 💌 Fixed Config: 🗹 I/O Type: Output 💌 Interrupt Type: Disabled	•		_
	к	Cancel	

Figure 39: CoreGPIO_OUT Configuration (all IOs have the same configuration)

3.3.3.9 IP Core CORESPI_0

Configurator					-	
CoreSPI Config	gurator					
licrosemi:DirectCore:COR	SPI:5.2.104					
Configuration						
APB Data Width: 🔿 8 📿	16 • 3	32				
SPI Configuration						
Mode: •	Motorola Mode	C TI Mode		Mode		
Frame Size (4-32): 8						
FIFO Depth (1-32): 32					_	
Clock Rate (0-255): 7					_	
Motorola Configuration	ode 0 C M	Mode 1 O N	1ode 2	O Mode 3		
Motorola Configuration Mode:	ode 0 C N	Mode 1 C N	1ode 2	C Mode 3		
Motorola Configuration Mode:	ode 0 C M	Mode 1 O M	lode 2	C Mode 3		
Motorola Configuration Mode: Mode:	ode 0 C M C Normal	Mode 1 O M	lode 2	C Mode 3		
Motorola Configuration Mode:	ode 0 C M G Normal	Mode 1 ON	lode 2	C Mode 3		
Motorola Configuration Mode:	ode 0 C M © Normal C D on Standard	Mode 1 C N	tode 2	C Mode 3		
Motorola Configuration Mode: Mode:	ode 0 C M C Normal C Standard	Mode 1 C M	iode 2 (C Mode 3		
Motorola Configuration Mode: Mo Keep SSEL active V TI/NSC Configuration Transfer Mode: Free running clock Jumbo frames NSC Specific Configuration Testbench: User V License: RTL	ode 0 C M C Normal C Standard	Mode 1 C M	iode 2	C Mode 3		

Figure 40: CORESPI_0 Configuration

3.3.3.10 IP Core COREI2C_0

oreI2C Configu	rator				
icrosemi:DirectCore:COREI2C:	7.2.101				
Configuration					
General:					
Number of I2C Channels: 1	Channel		•		
Operating Mode:	ull Master RX/TX, Slave RX/TX Mode	es (Largest Tile Count)	•		
SMBus or IPMI Logic Options:					_
Generate SMBus Logic (Regist	ter, Timeouts, Bus Reset, and Aler	t/Suspend Signals): 🗌			
Generate IPMI Logic (Register	r, and 3 ms SCL Low Timeout):				
PCLK Frequency in MHz (Requ	uired to Calibrate Timeout Counter	s): 30		_	
Baud Rate Options (for Tile Count	Reduction):				
Fixed Baud Rate:	Fixed Baud Rate Value: PCLK free	quency / 256 💌			
Enable BCLK Signal: 🔽					
Slave Address Options (for Tile Co	unt Reduction and to Enable 2nd A	Address Decode Value):			_
Fixed Slave0 Address:					
Fixed Slave0 Address Value:	0×0				
Enable 2nd Address Decode ((Slave 1 Address):				
Fixed Slave1 Address:	Г				
	0×0				
Fixed Slave1 Address Value:					
Fixed Slave 1 Address Value: Spike/Glitch Suppression Option:					
Fixed Slave 1 Address Value: Spike/Glitch Suppression Option: — Supression Width:	5 PC	LK Periods		•	
Fixed Slave 1 Address Value: Spike/Glitch Suppression Option: Supression Width: General:	5 PC	LK Periods		•	
Fixed Slave 1 Address Value: Spike/Glitch Suppression Option: – Supression Width: General: Testbench:	5 PC	LK Periods		•	

Figure 41: COREI2C_0 Configuration

3.3.3.11 IP Core COREI2C_1

oreI2C Config	urator						
icrosemi:DirectCore:CORE	2C:7.2.101						
Configuration							
General:							
Number of I2C Channels:	1 Channel				•		
Operating Mode:	Full Master RX/TX,	Slave RX/T)	(Modes (Large	st Tile Count)	•		
SMBus or IPMI Logic Options: -							
Generate SMBus Logic (Re	egister, Timeouts, Bi	us Reset, an	d Alert/Suspen	d Signals): 🗌			
Generate IPMI Logic (Reg	ister, and 3 ms SCL	Low Timeout	:):				
PCLK Frequency in MHz (F	Required to Calibrate	e Timeout Co	unters):	30		_	
Baud Rate Options (for Tile Co	unt Reduction):						
Fixed Baud Rate:	Fixed Baud Rate	Value: PO	LK frequency /	256 💌			
Enable BCLK Signal: 🔽							
Slave Address Options (for Tile	Count Reduction a	nd to Enable	2nd Address D	ecode Value):			
Fixed Slave0 Address:							
Fixed Slave0 Address Valu	ie:	0x0					
Enable 2nd Address Deco	de (Slave1 Address)	:					
Fixed Slave 1 Address:		Г					
Fixed Slave 1 Address Valu	Je:	0x0					
Spike/Glitch Suppression Optio	n:						
Supression Width:			5 PCLK Period	S		•	•
General:							
Testbench:			User				•

Figure 42: COREI2C_1 Configuration

3.3.4 Smart Design video_isp_pipe



Figure 43: SmartDesign video_isp_pipe

3.3.4.1 IP Core Bayer_IP0_0

Configurator		_	_		\times
Bayer Interpola	tion C	onfig	ura	ator	
Microsemi:SolutionCore:Baye	erConversio	onTop:2.0.0)		
Configuration					
g_DATAWIDTH:	8				
g_X_RES_WIDTH:	11				
g_DISPLAY_RESOLUTION:	1280				
g_VERT_DISPLAY_RESOLUTION:	720				
testbench:	User	•			
License:	Obfuscated				
Help 🔻		ОК		Cano	el

Figure 44: Bayer_IP0_0 Configuration

3.3.4.2 IP Core RGB2YCbCr_IP0_0

Configurator	_		
		ator	
Configuration	GD21CDCF.3.0.1		
G_RGB_DATA_BIT_WIDTH:	8 💌		
G_YCbCr_DATA_BIT_WIDTH	8 💌		
testbench:	User 💌		
License:	Obfuscated		
Help 🔻	ОК	Cancel	

Figure 45: RGB2YCbCr_IP0_0 Configuration

3.3.4.3 IP Core ImageEdgeDetection_IP0_0

Configurator		_		×
Image Edge De	etection Co	nfiau	irato	r
Microsemi:SolutionCore:Ima	ageEdgeDetection:2	2.0.0		-
Configuration				
g_DATAWIDTH:	8	_		
g_X_RES_WIDTH:	11	-		
g_DISPLAY_RESOLUTION:	1280			
g_VERT_DISPLAY_RESOLUTION	: 720			
testbench:	User	•		
License:	Obfuscated			
Help 🔻		ОК	Cano	:el

Figure 46: ImageEdgeDetection_IP0_0 Configuration

3.3.4.4 IP Core YCbCr2RGB_IP0_0

Configurator	_			\times
YCbCr to RGB	Config	ura 0.1	ator	
Configuration				
G_RGB_DATA_BIT_WIDTH:	8 💌			
G_YCbCr_DATA_BIT_WIDTH:	8 💌			
testbench:	User 💌			
License:	Obfuscated			
Help 🔻	ОК		Cancel	

Figure 47: YCbCr2RGB_IP0_0 Configuration

3.3.4.5 IP Core Alpha_Blending_Control_IP0_0

Configurator	_			×
Alpha Blending Co	onfigurat	tor		
Microsemi:SolutionCore:alpha_t	olend_control:2.	0.0		
Configuration				
g_IMAGE_DATAWIDTH:	32			
g_FRAME_DATAWIDTH:	24			
g_OUTPUT_CHANNEL_DATAWIDTH:	24			
g_IMAGE_BUFFER_AWIDTH:	11			
g_FRAME_BUFFER_AWIDTH:	11	_		
g_IMAGE_X_Y_DATAWIDTH:	11			
g_FRAME_X_Y_DATAWIDTH:	11	_		
testbench:	User	•		
License:	Obfuscated			
Help 🔻	ОК		Cancel	

Figure 48: Alpha_Blending_Control_IP0_0 Configuration

3.3.4.6 IP Core RGB2YCbCr_IP1_0

Configurator	– 🗆 X
RGB To YCbCr	Configurator
Microsemi:SolutionCore:R	GB2YCbCr:3.0.1
Configuration	
G_RGB_DATA_BIT_WIDTH:	8 💌
G_YCbCr_DATA_BIT_WIDTH:	8 💌
testbench:	User 💌
License:	Obfuscated
Help 🔻	OK Cancel
	1

Figure 49: RGB2YCbCr_IP1_0 Configuration

3.3.4.7 IP Core ImageSharpenFilter_IP0_0

Configurator	- 🗆 X
Image Sharper	n Configurator
Microsemi:SolutionCore:Ima	ageSharpenFilter:2.0.0
Configuration	1
g_DATAWIDTH:	24
g_X_RES_WIDTH:	11
g_DISPLAY_RESOLUTION:	1280
g_VERT_DISPLAY_RESOLUTION	ł: 720
testbench:	User
License:	Obfuscated
Help 🔻	OK Cancel

Figure 50: ImageSharpenFilter_IP0_0 Configuration

3.4 Running the Design

The design uses a MIV processor. The release is programmed in NVM.

The software project can be found in the MiV_Workspace

If programmed correctly, the camera image appears on the monitor after powering the board.

Use the GUI to adjust the image enhancements or run the edge Detection.

😂 PolarFire Im	naging/Video Demo v1.0	
Imaging/Video GUI		
Demo Select	tion Camera Sensor Demo	
Image Enhancements		
Brig	ightness	
-128	intrast	
-128	127	
Sa	aturation	
-128	Hue 127	
0		
-180	180	
sn	arpness	
C Mic	crosemi Exit	

Figure 51: Imaging/Video GUI