Five Years Out

Everest-MIPI CSI-2 - Demo

Getting Started

Project: Everest-MIPI-CSI-2-Demo Getting Started	created:	S. Rieche	Date	2019-03-20
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Arrow Central Europe GmbH	Version:	1.1	Page 1 of 50	

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1. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Updated for Libero 12.4.

1.2 Revision 1.0

Revision 1.0 is the first publication of this document.

2. Getting Started

This demo design includes a video and imaging demo using the PolarFire Everest DEV Board and Video MIPI CSI-2 Daughter Card. Using the on board HDMI port to print a Full HD (1920x1080@60Hz) on a HDMI monitor.
Prerequisites
For the Everest MIPC-CSI-2 Demo the following is needed:

Item	**Quantity**
Everest DEV Board	1
12 V / 5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for UART / Programming interface to PC	1
HDMI cable	1
HDMI monitor (1920x1080@60Hz)	1
MIPI CSI-2 Daughter Card	1
Image sensor module LI-AR0330-MIPI v1.1	1
Image sensor ribbon cable	1
Free one-year Libero Silver software license	1

Note 1: The Everest DEV Board offers an on-board FlashPro5 programmer, which can be used to program and debug with Identify, SmartDebug and embedded application software using SoftConsole.

Note 2: The descripted design is suitable for Everest Dev Board Rev PROTO, A and B.

2.1 Handling the Board

Pay attention to the following points while handling or operating the board:

Handle the board with electrostatic discharge (ESD) precautions to avoid damage.

For information about ESD precautions see https://www.microsemi.com/documentportal/doc_view/126483-esd-appnote.

2.2 Board-Setup Revision PROTO

2.2.1 Toggle-Switch S1 – PCIe

Warning: S1-1 and S1-2 must not be at position on at the same time!

SWITCH ON	**PCIe LANES**
S1-1	x1
S1-2	x4

2.2.2 Toggle -Switch S5 – SC SPI-Flash enable

Warning: S5-1 and S5-2 must not be at position on at the same time!

SWITCH ON	**SC SPI-FLASH**
S5-1	ENABLE
S5-2	DISABLE

2.2.3 DIP-Switch S8 – FMC Voltage Selector

Warning: S8-1 to S8-4 must not be at position on at the same time!

SWITCH ON	**FMC VOLTAGE**
S8-1	3.3 V
S8-2	2.5 V
S8-3	1.8 V
S8-4	undefined (not connected)

2.2.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

Warning: S9-1 and S9-2 must not be at position on at the same time!

SWITCH ON	**VDDAUX2 & VDDAUX5**
S9-1	2.5 V
S9-2	FMC voltage

Use the marked settings for the demo.

2.3 Board-Setup Revision A and B

2.3.1 Toggle-Switch S1 – PCIe

SWITCH	PCIe LANES
S1-1 (marking)	x4
S1-2	x1

2.3.2 Toggle -Switch S5 – SC SPI-Flash enable

SWITCH	SC SPI-FLASH
S5-1 (marking)	DISABLE
S5-2	ENABLE

2.3.3 DIP-Switch S8 – FMC Voltage Selector

SWITCH	FMC VOLTAGE
S8-1 off, S8-2 off	1.8 V
S8-1 on, S8-2 off	2.5 V
S8-1 off, S8-2 on	undefined (not recommended)
S8-1 on, S8-2 on	3.3 V

2.3.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

SWITCH	VDDAUX2 & VDDAUX5
S9-1 (marking)	2.5 V
S9-2	FMC voltage

Use the marked settings for the demo.

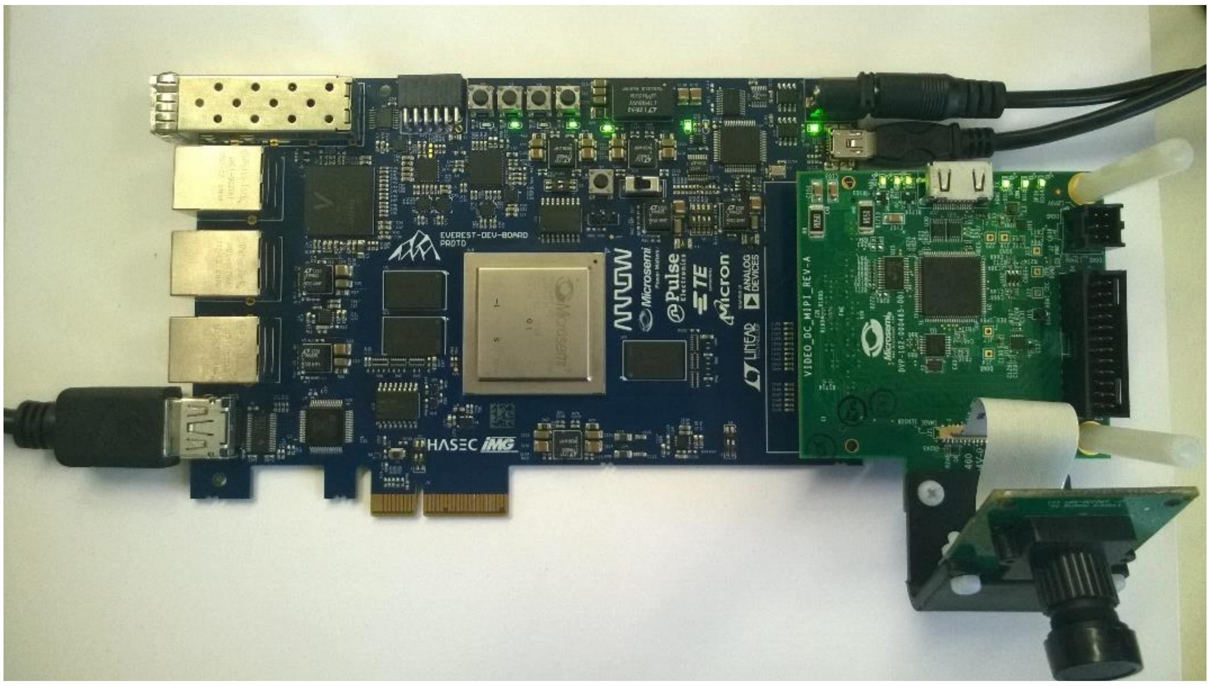


Figure 1: Everest Board + MIPI CSI-2 Daughter Card

2.4 Powering up the Board

The Everest DEV Board is powered up using either the 12 V DC jack or the PCIe connector. For programming connect it although with your computer using USB mini B connector J9. A HDMI monitor should be connected with an appropriate cable via HDMI connector J2.

3. Demo Design

3.1 Prerequisites

Table 1: Software

Software	Version
Libero SoC PolarFire	V12.0
Synplify Pro	L2017.09M-SP1-1
FlashPro PolarFire	V2.0

Download the Video Demo GUI from
http://soc.microsemi.com/download/rsc/?f=mpf_dg0807_liberosocpolarfirev2p0_gui

Before you start you have to make sure, that all cores are downloaded to your local vault.

3.2 Design Implementation

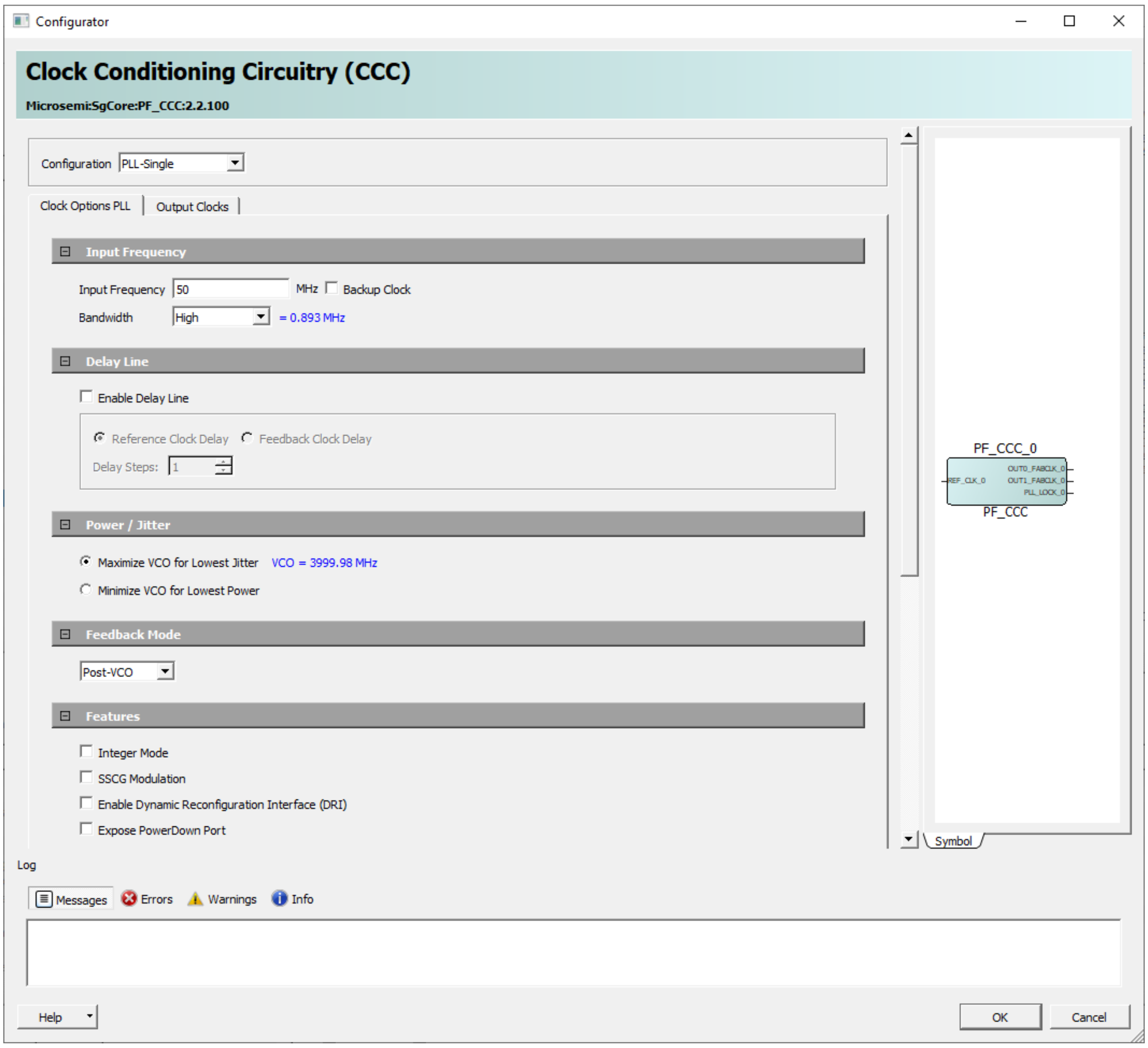
The design is already fully implemented and ready to be programmed on the Everest Board. The board has to be connected with the power supply and to the PC with the USB cable. All drivers have to be installed (which should happen automatically when plugged in the first time) To program the design, there are two possibilities:

- Programming via Libero PolarFire SoC: Programming is started with the “Run PROGRAM Action” Button in the Design Flow Pane
- Programming via FlashPro Software: There is a STAPL-File (“<Design Directory>\designer\PF_AR0330_CAM_TOP\export\PF_AR0330_CAM_TOP_ADV.stp”) which can be programmed with the FlashPro Software. A new FlashPro project has to be generated and the programming file loaded into.

3.3 IP Core Configuration

3.3.1 Smart Design PF_AR0330_CAM_TOP

3.3.1.1 IP Core PF_CCC_2_0



Configurator

Clock Conditioning Circuitry (CCC)

Microsemi:SgCore:PF_CCC:2.2.100

Configuration: PLL-Single

Clock Options PLL | Output Clocks

Input Frequency

Input Frequency: 50 MHz ☐ Backup Clock

Bandwidth: High = 0.893 MHz

Delay Line

☐ Enable Delay Line

● Reference Clock Delay ○ Feedback Clock Delay

Delay Steps: 1

Power / Jitter

● Maximize VCO for Lowest Jitter VCO = 3999.98 MHz

○ Minimize VCO for Lowest Power

Feedback Mode

Post-VCO

Features

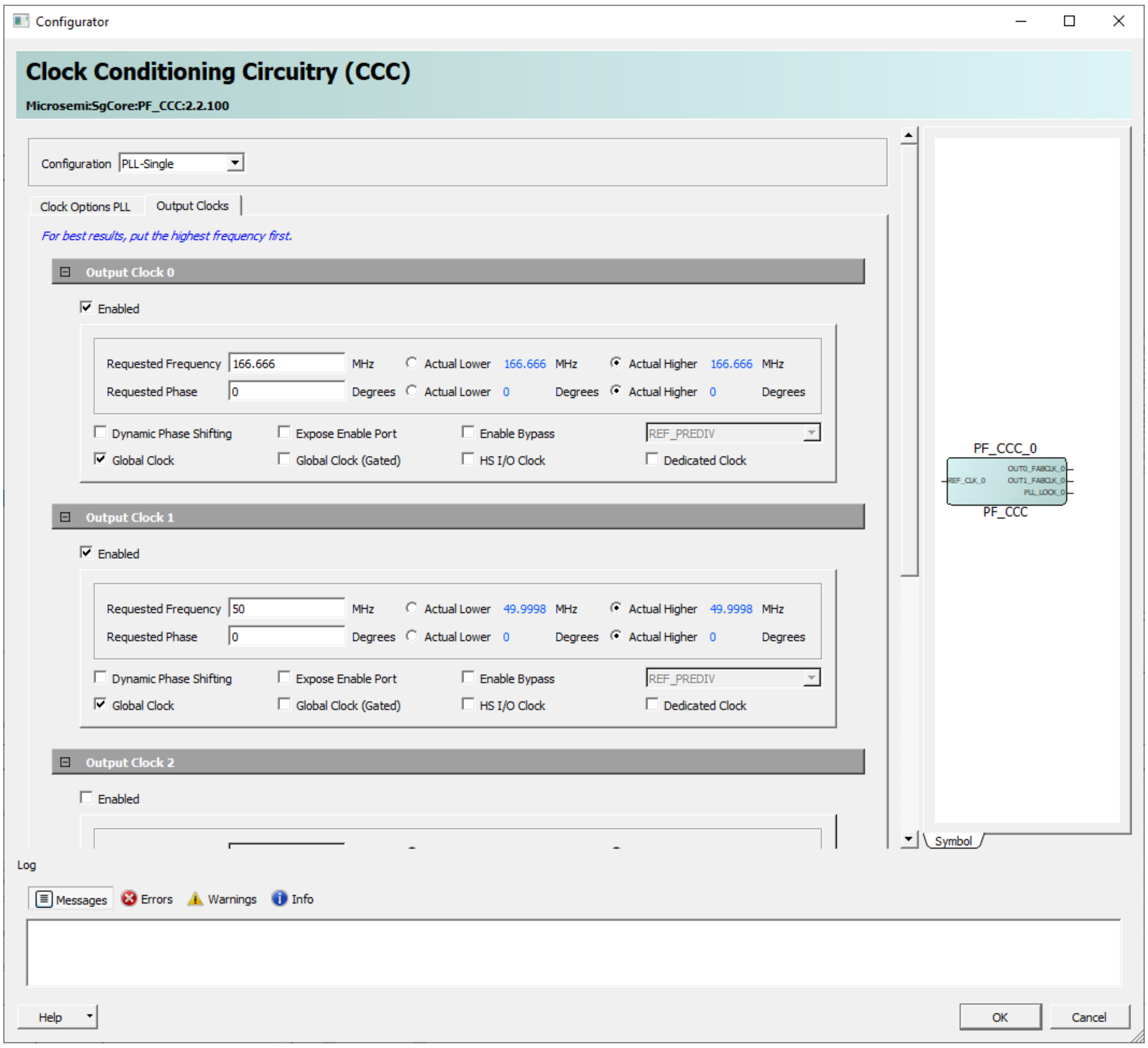
☐ Integer Mode

☐ SSCG Modulation

☐ Enable Dynamic Reconfiguration Interface (DRI)

☐ Expose PowerDown Port

Figure 2: PF_CCC_2_0 Clock Options PLL



Configurator

Clock Conditioning Circuitry (CCC)

Microsemi:SgCore:PF_CCC:2.2.100

Configuration: PLL-Single

Clock Options PLL | Output Clocks

For best results, put the highest frequency first.

Output Clock 0

☑ Enabled

Requested Frequency: 166.666 MHz ○ Actual Lower 166.666 MHz ● Actual Higher 166.666 MHz
Requested Phase: 0 Degrees ○ Actual Lower 0 Degrees ● Actual Higher 0 Degrees

☐ Dynamic Phase Shifting ☐ Expose Enable Port ☐ Enable Bypass REF_PREDIV
☑ Global Clock ☐ Global Clock (Gated) ☐ HS I/O Clock ☐ Dedicated Clock

Output Clock 1

☑ Enabled

Requested Frequency: 50 MHz ○ Actual Lower 49.9998 MHz ● Actual Higher 49.9998 MHz
Requested Phase: 0 Degrees ○ Actual Lower 0 Degrees ● Actual Higher 0 Degrees

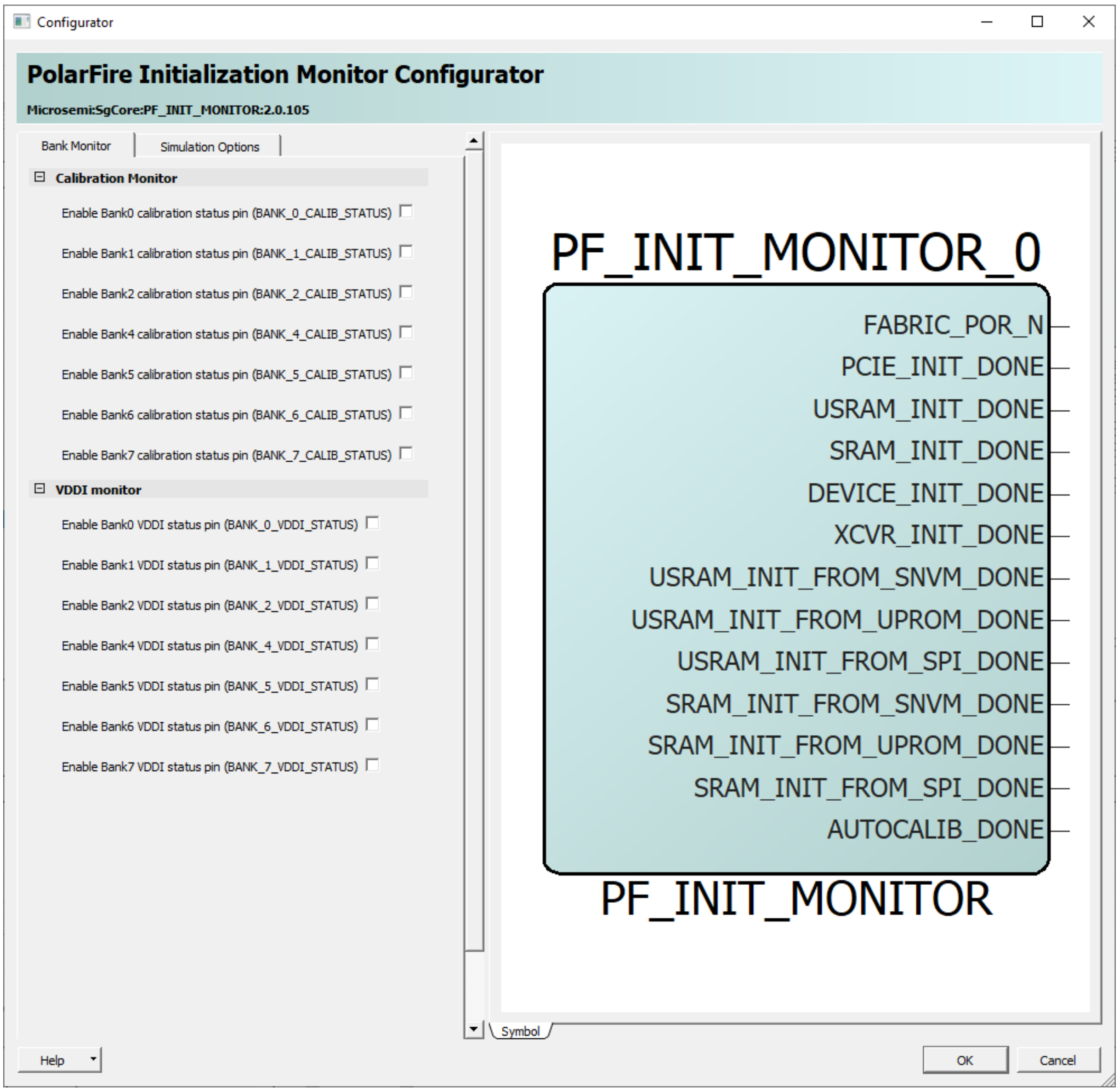
☐ Dynamic Phase Shifting ☐ Expose Enable Port ☐ Enable Bypass REF_PREDIV
☑ Global Clock ☐ Global Clock (Gated) ☐ HS I/O Clock ☐ Dedicated Clock

Output Clock 2

☐ Enabled

Figure 3: PF_CCC_2_0 Output Clocks

3.3.1.2 IP Core PF_INIT_MONITOR_0


Configurator

PolarFire Initialization Monitor Configurator

Microsemi:SgCore:PF_INIT_MONITOR:2.0.105

Bank Monitor | Simulation Options

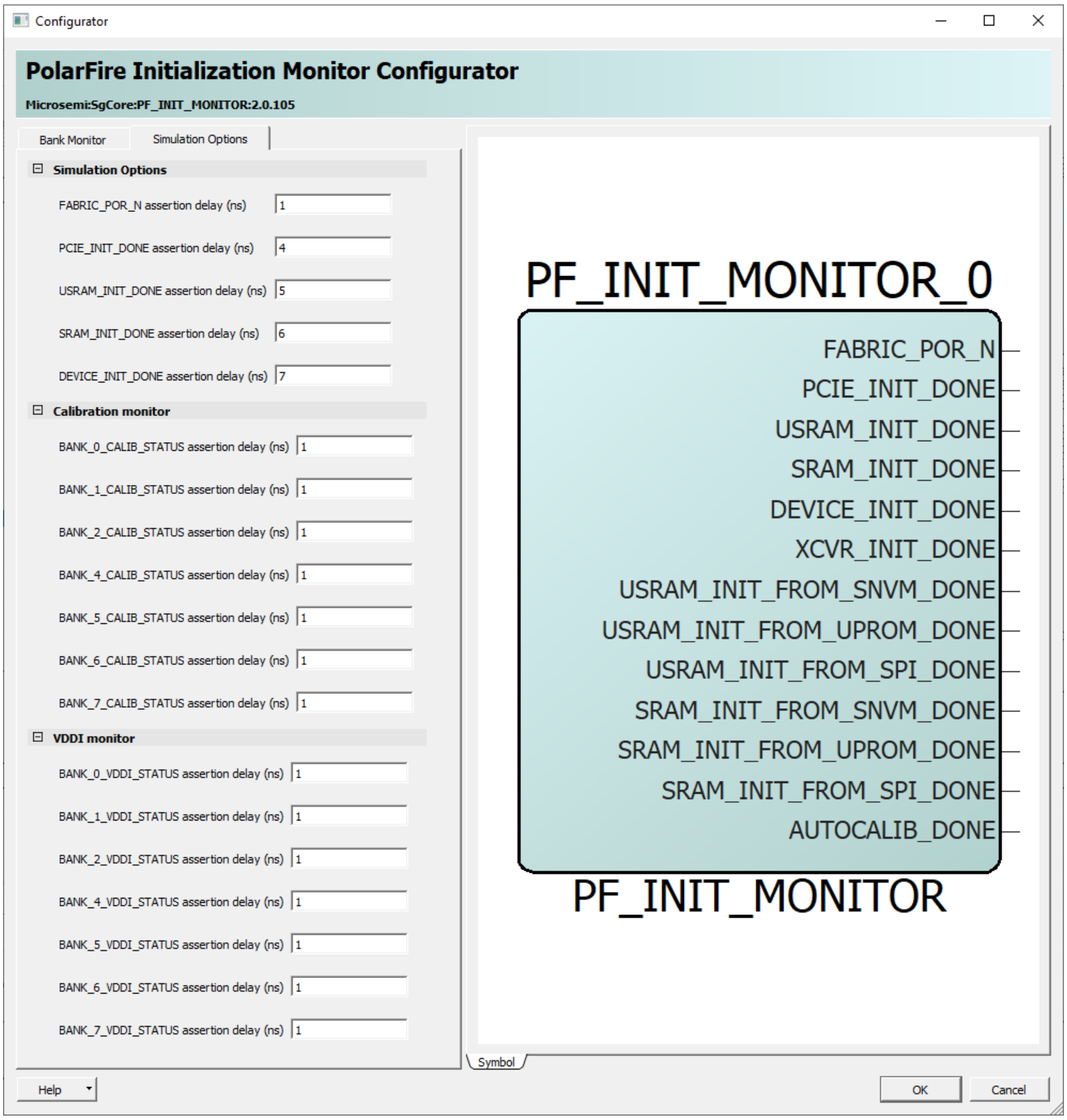
Calibration Monitor

Enable Bank0 calibration status pin (BANK_0_CALIB_STATUS) ☐
Enable Bank1 calibration status pin (BANK_1_CALIB_STATUS) ☐
Enable Bank2 calibration status pin (BANK_2_CALIB_STATUS) ☐
Enable Bank4 calibration status pin (BANK_4_CALIB_STATUS) ☐
Enable Bank5 calibration status pin (BANK_5_CALIB_STATUS) ☐
Enable Bank6 calibration status pin (BANK_6_CALIB_STATUS) ☐
Enable Bank7 calibration status pin (BANK_7_CALIB_STATUS) ☐

VDDI monitor

Enable Bank0 VDDI status pin (BANK_0_VDDI_STATUS) ☐
Enable Bank1 VDDI status pin (BANK_1_VDDI_STATUS) ☐
Enable Bank2 VDDI status pin (BANK_2_VDDI_STATUS) ☐
Enable Bank4 VDDI status pin (BANK_4_VDDI_STATUS) ☐
Enable Bank5 VDDI status pin (BANK_5_VDDI_STATUS) ☐
Enable Bank6 VDDI status pin (BANK_6_VDDI_STATUS) ☐
Enable Bank7 VDDI status pin (BANK_7_VDDI_STATUS) ☐

Figure 4: PF_INIT_Monitor_0 Bank Monitor


Configurator

PolarFire Initialization Monitor Configurator

Microsemi:SgCore:PF_INIT_MONITOR:2.0.105

Bank Monitor | Simulation Options

Simulation Options

FABRIC_POR_N assertion delay (ns)	1
PCIE_INIT_DONE assertion delay (ns)	4
USRAM_INIT_DONE assertion delay (ns)	5
SRAM_INIT_DONE assertion delay (ns)	6
DEVICE_INIT_DONE assertion delay (ns)	7

Calibration monitor

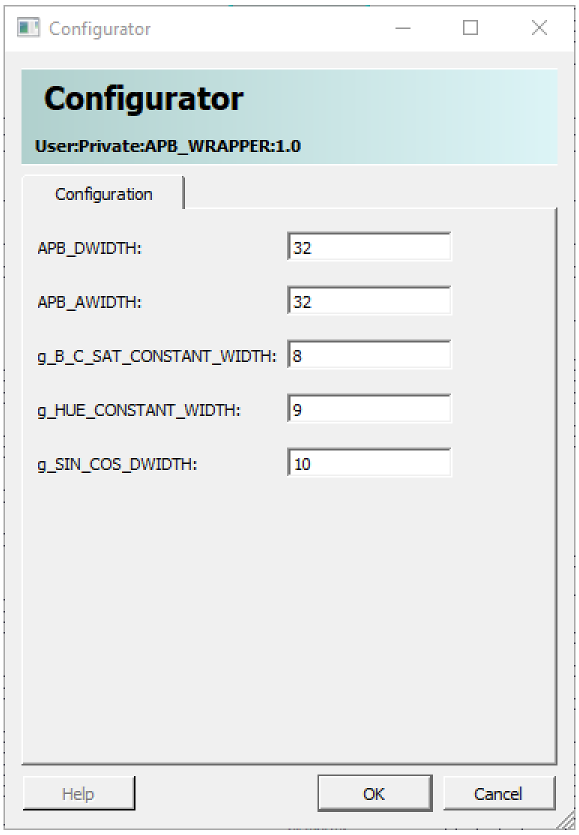
BANK_0_CALIB_STATUS assertion delay (ns)	1
BANK_1_CALIB_STATUS assertion delay (ns)	1
BANK_2_CALIB_STATUS assertion delay (ns)	1
BANK_4_CALIB_STATUS assertion delay (ns)	1
BANK_5_CALIB_STATUS assertion delay (ns)	1
BANK_6_CALIB_STATUS assertion delay (ns)	1
BANK_7_CALIB_STATUS assertion delay (ns)	1

VDDI monitor

BANK_0_VDDI_STATUS assertion delay (ns)	1
BANK_1_VDDI_STATUS assertion delay (ns)	1
BANK_2_VDDI_STATUS assertion delay (ns)	1
BANK_4_VDDI_STATUS assertion delay (ns)	1
BANK_5_VDDI_STATUS assertion delay (ns)	1
BANK_6_VDDI_STATUS assertion delay (ns)	1
BANK_7_VDDI_STATUS assertion delay (ns)	1

Figure 5: PF_INIT_Monitor_0 Simulation Options

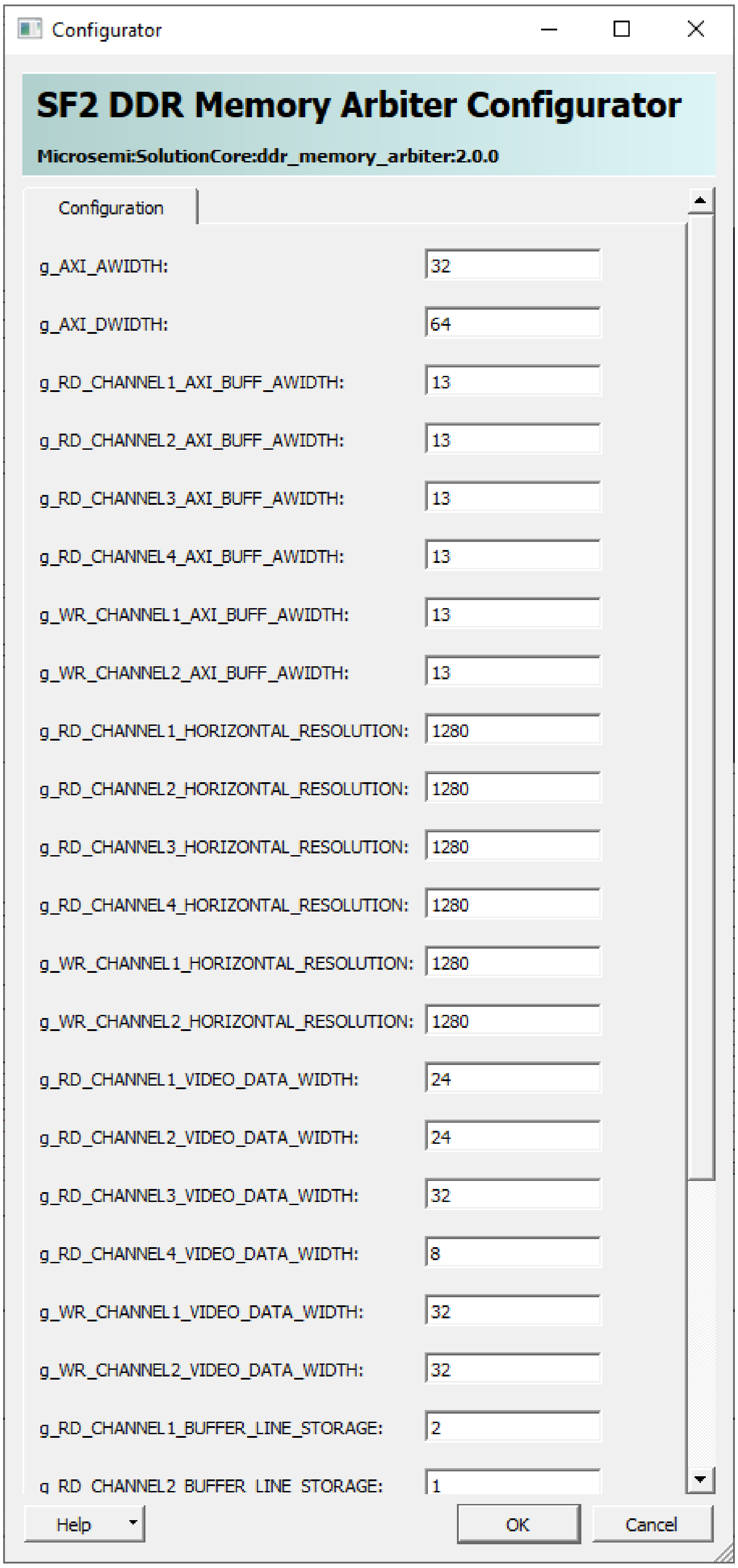
3.3.1.3 IP Core APB_WRAPPER_0



APB_DWIDTH:	32
APB_AWIDTH:	32
g_B_C_SAT_CONSTANT_WIDTH:	8
g_HUE_CONSTANT_WIDTH:	9
g_SIN_COS_DWIDTH:	10

Figure 6: APB_WRAPPER_0 Configuration

3.3.1.4 IP Core DDR_Memory_Arbiter_IP0_0

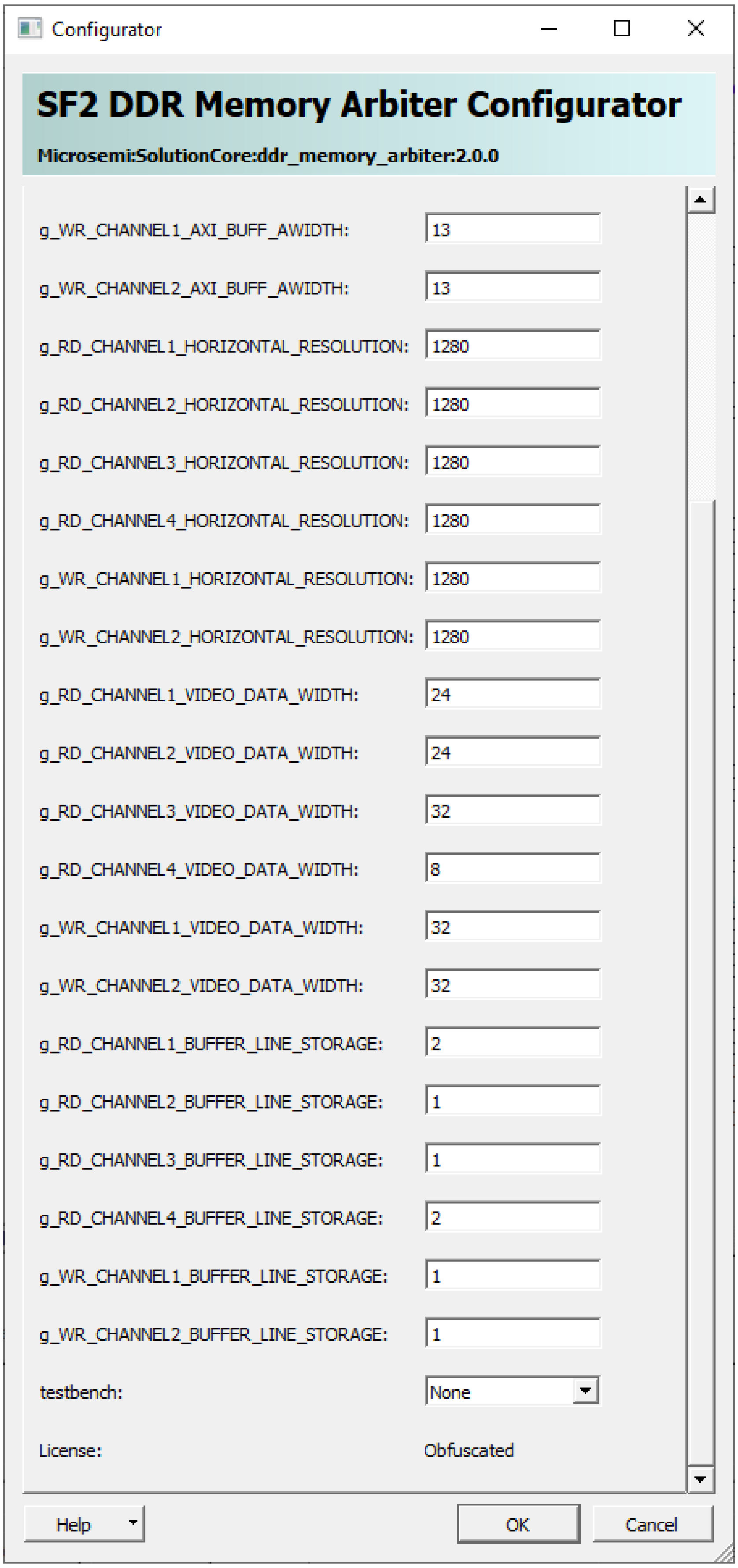


SF2 DDR Memory Arbiter Configurator

Microsemi:SolutionCore:ddr_memory_arbiter:2.0.0

g_AXI_AWIDTH:	32
g_AXI_DWIDTH:	64
g_RD_CHANNEL1_AXI_BUFF_AWIDTH:	13
g_RD_CHANNEL2_AXI_BUFF_AWIDTH:	13
g_RD_CHANNEL3_AXI_BUFF_AWIDTH:	13
g_RD_CHANNEL4_AXI_BUFF_AWIDTH:	13
g_WR_CHANNEL1_AXI_BUFF_AWIDTH:	13
g_WR_CHANNEL2_AXI_BUFF_AWIDTH:	13
g_RD_CHANNEL1_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL2_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL3_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL4_HORIZONTAL_RESOLUTION:	1280
g_WR_CHANNEL1_HORIZONTAL_RESOLUTION:	1280
g_WR_CHANNEL2_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL1_VIDEO_DATA_WIDTH:	24
g_RD_CHANNEL2_VIDEO_DATA_WIDTH:	24
g_RD_CHANNEL3_VIDEO_DATA_WIDTH:	32
g_RD_CHANNEL4_VIDEO_DATA_WIDTH:	8
g_WR_CHANNEL1_VIDEO_DATA_WIDTH:	32
g_WR_CHANNEL2_VIDEO_DATA_WIDTH:	32
g_RD_CHANNEL1_BUFFER_LINE_STORAGE:	2
g_RD_CHANNEL2_BUFFER_LINE_STORAGE:	1

Figure 7: DDR_Memory_Arbiter_IP0 Configuration



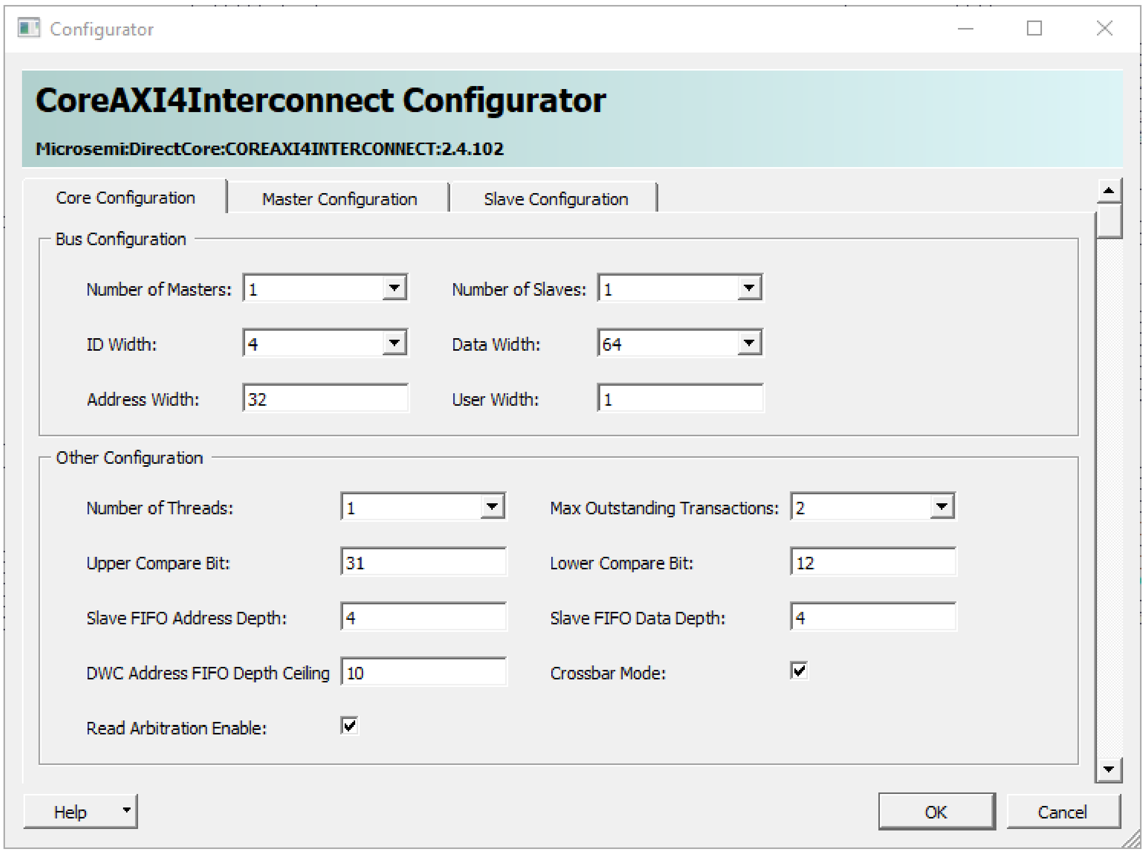
SF2 DDR Memory Arbiter Configurator

Microsemi:SolutionCore:ddr_memory_arbiter:2.0.0

g_WR_CHANNEL1_AXI_BUFF_AWIDTH:	13
g_WR_CHANNEL2_AXI_BUFF_AWIDTH:	13
g_RD_CHANNEL1_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL2_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL3_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL4_HORIZONTAL_RESOLUTION:	1280
g_WR_CHANNEL1_HORIZONTAL_RESOLUTION:	1280
g_WR_CHANNEL2_HORIZONTAL_RESOLUTION:	1280
g_RD_CHANNEL1_VIDEO_DATA_WIDTH:	24
g_RD_CHANNEL2_VIDEO_DATA_WIDTH:	24
g_RD_CHANNEL3_VIDEO_DATA_WIDTH:	32
g_RD_CHANNEL4_VIDEO_DATA_WIDTH:	8
g_WR_CHANNEL1_VIDEO_DATA_WIDTH:	32
g_WR_CHANNEL2_VIDEO_DATA_WIDTH:	32
g_RD_CHANNEL1_BUFFER_LINE_STORAGE:	2
g_RD_CHANNEL2_BUFFER_LINE_STORAGE:	1
g_RD_CHANNEL3_BUFFER_LINE_STORAGE:	1
g_RD_CHANNEL4_BUFFER_LINE_STORAGE:	2
g_WR_CHANNEL1_BUFFER_LINE_STORAGE:	1
g_WR_CHANNEL2_BUFFER_LINE_STORAGE:	1
testbench:	None
License:	Obfuscated

Figure 8: DDR_Memory_Arbiter_IP0 Configuration cont. ...

3.3.1.5 IP Core CoreAXI4Interconnect_0



CoreAXI4Interconnect Configurator

Microsemi:DirectCore:COREAXI4INTERCONNECT:2.4.102

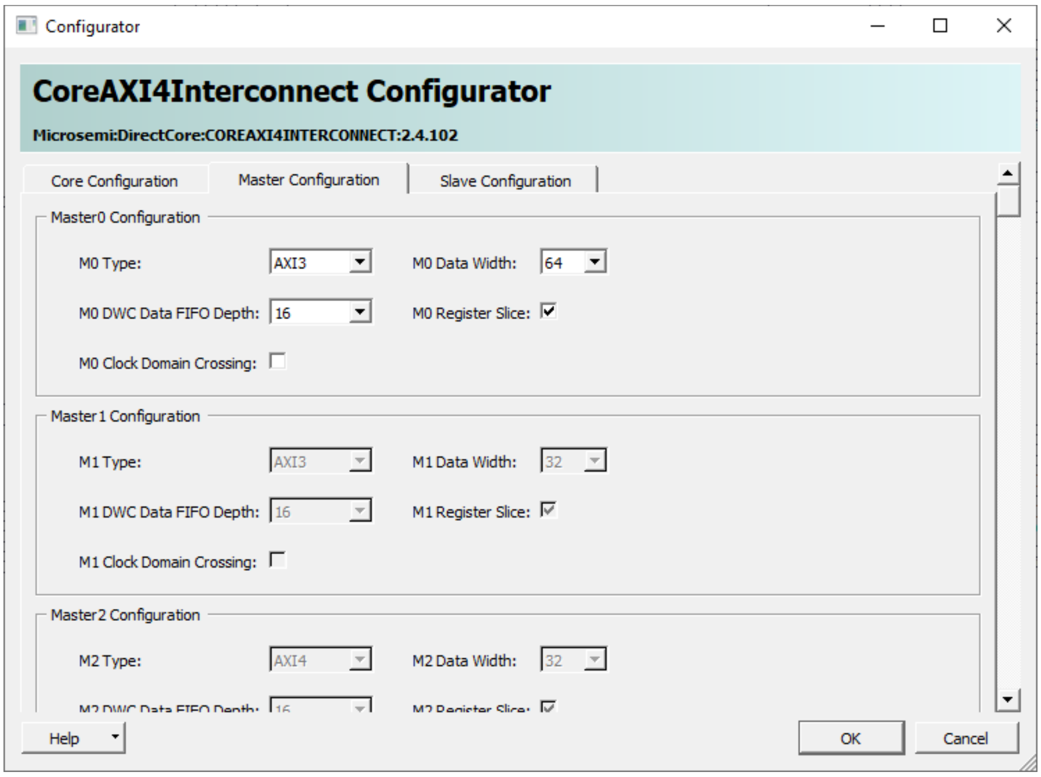
Bus Configuration

Number of Masters:	1	Number of Slaves:	1
ID Width:	4	Data Width:	64
Address Width:	32	User Width:	1

Other Configuration

Number of Threads:	1	Max Outstanding Transactions:	2
Upper Compare Bit:	31	Lower Compare Bit:	12
Slave FIFO Address Depth:	4	Slave FIFO Data Depth:	4
DWC Address FIFO Depth Ceiling	10	Crossbar Mode:	✓
Read Arbitration Enable:	✓		

Figure 9: CoreAXI4Interconnect_0 Core Configuration



CoreAXI4Interconnect Configurator

Microsemi:DirectCore:COREAXI4INTERCONNECT:2.4.102

Master0 Configuration

M0 Type:	AXI3	M0 Data Width:	64
M0 DWC Data FIFO Depth:	16	M0 Register Slice:	✓
M0 Clock Domain Crossing:	☐		

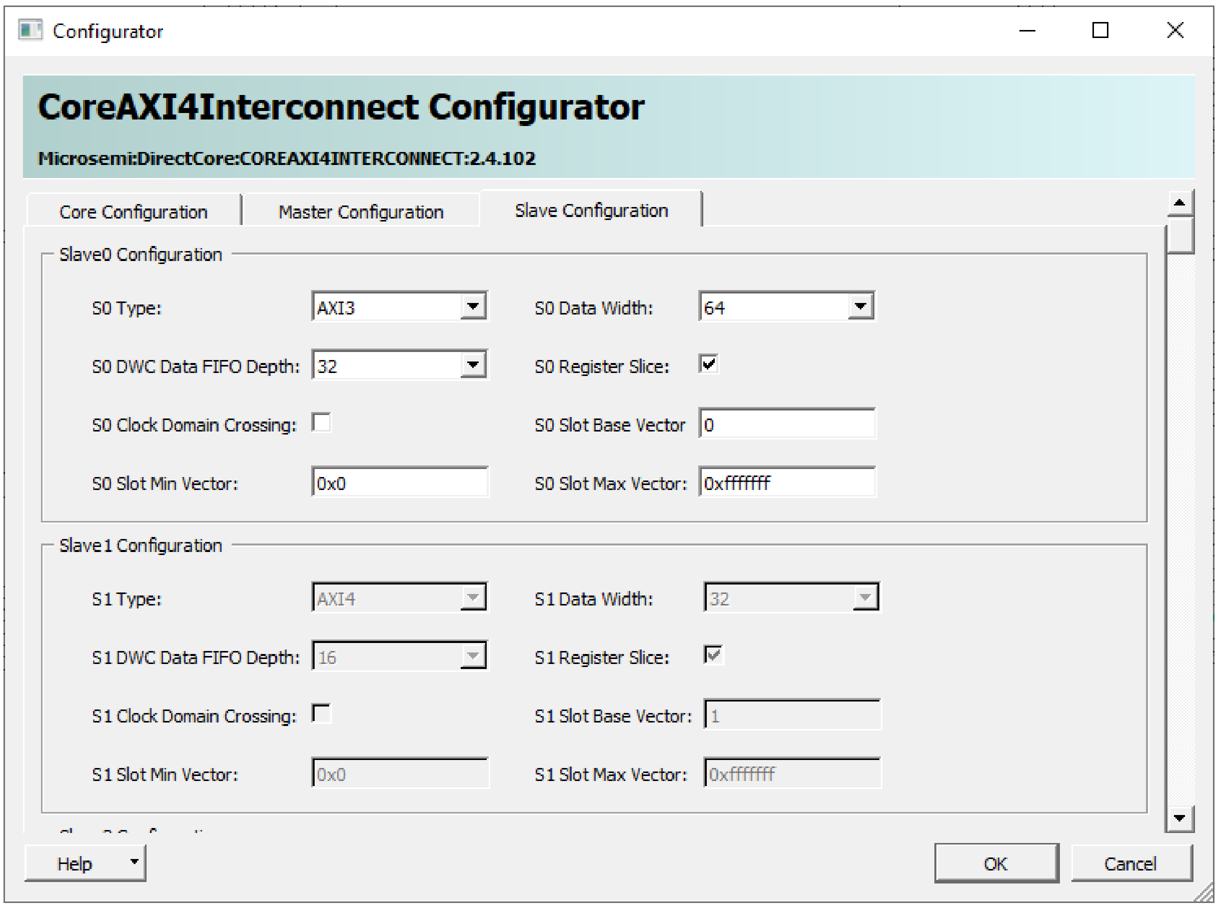
Master1 Configuration

M1 Type:	AXI3	M1 Data Width:	32
M1 DWC Data FIFO Depth:	16	M1 Register Slice:	✓
M1 Clock Domain Crossing:	☐		

Master2 Configuration

M2 Type:	AXI4	M2 Data Width:	32
M2 DWC Data FIFO Depth:	16	M2 Register Slice:	✓

Figure 10: CoreAXI4Interconnect_0 Master Configuration


Configurator
CoreAXI4Interconnect Configurator
Microsemi:DirectCore:COREAXI4INTERCONNECT:2.4.102
Core Configuration
Master Configuration
Slave Configuration
Help
OK
Cancel

Slave0 Configuration

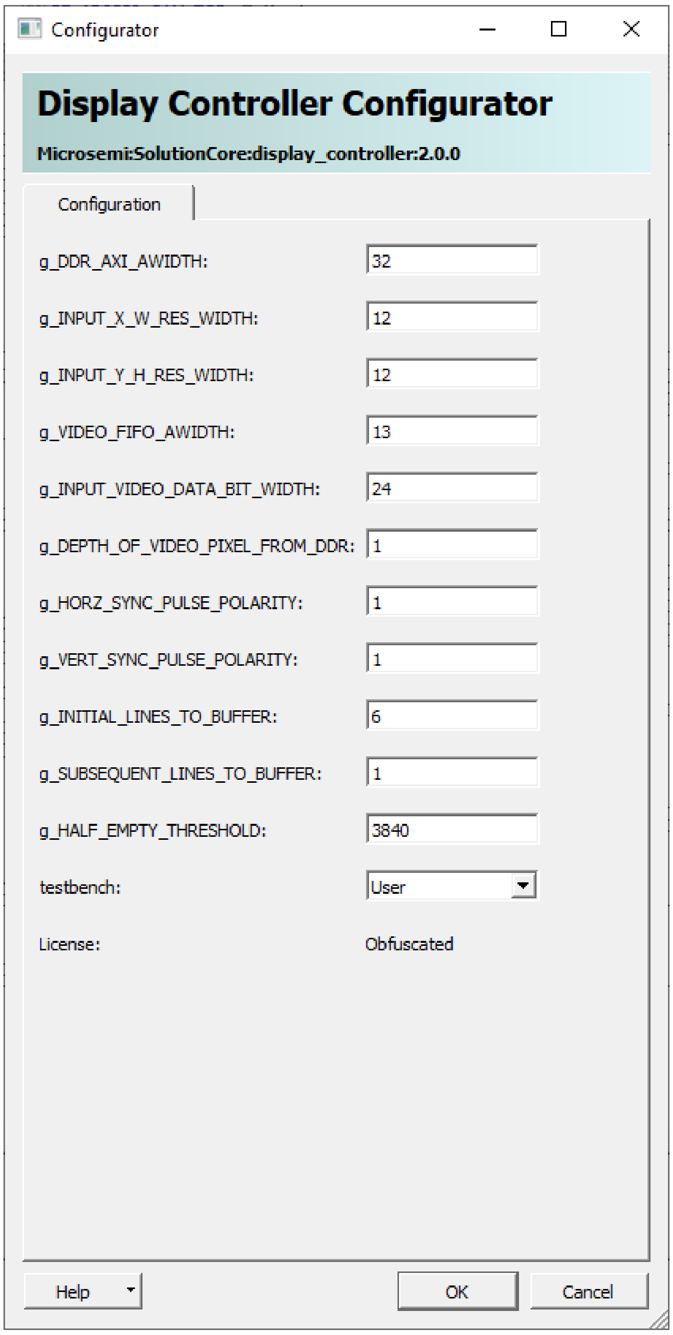
S0 Type:	AXI3	S0 Data Width:	64
S0 DWC Data FIFO Depth:	32	S0 Register Slice:	✓
S0 Clock Domain Crossing:	☐	S0 Slot Base Vector	0
S0 Slot Min Vector:	0x0	S0 Slot Max Vector:	0xfffffff

Slave1 Configuration

S1 Type:	AXI4	S1 Data Width:	32
S1 DWC Data FIFO Depth:	16	S1 Register Slice:	✓
S1 Clock Domain Crossing:	☐	S1 Slot Base Vector:	1
S1 Slot Min Vector:	0x0	S1 Slot Max Vector:	0xfffffff

Figure 11: CoreAXI4Interconnect_0 Slave Configuration

3.3.1.6 IP Core Display_Cntrll_0



Display Controller Configurator

Microsemi:SolutionCore:display_controller:2.0.0

g_DDR_AXI_AWIDTH:	32
g_INPUT_X_W_RES_WIDTH:	12
g_INPUT_Y_H_RES_WIDTH:	12
g_VIDEO_FIFO_AWIDTH:	13
g_INPUT_VIDEO_DATA_BIT_WIDTH:	24
g_DEPTH_OF_VIDEO_PIXEL_FROM_DDR:	1
g_HORZ_SYNC_PULSE_POLARITY:	1
g_VERT_SYNC_PULSE_POLARITY:	1
g_INITIAL_LINES_TO_BUFFER:	6
g_SUBSEQUENT_LINES_TO_BUFFER:	1
g_HALF_EMPTY_THRESHOLD:	3840
testbench:	User
License:	Obfuscated

Figure 12: Display_Cntrll_0 Configuration

3.3.1.7 IP Core DisplayEnhancement_0_0

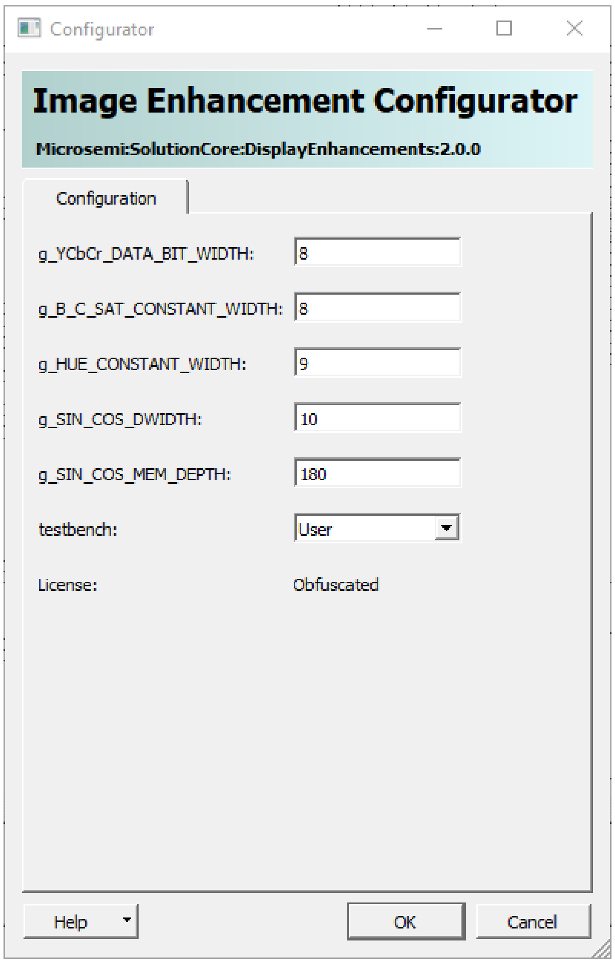


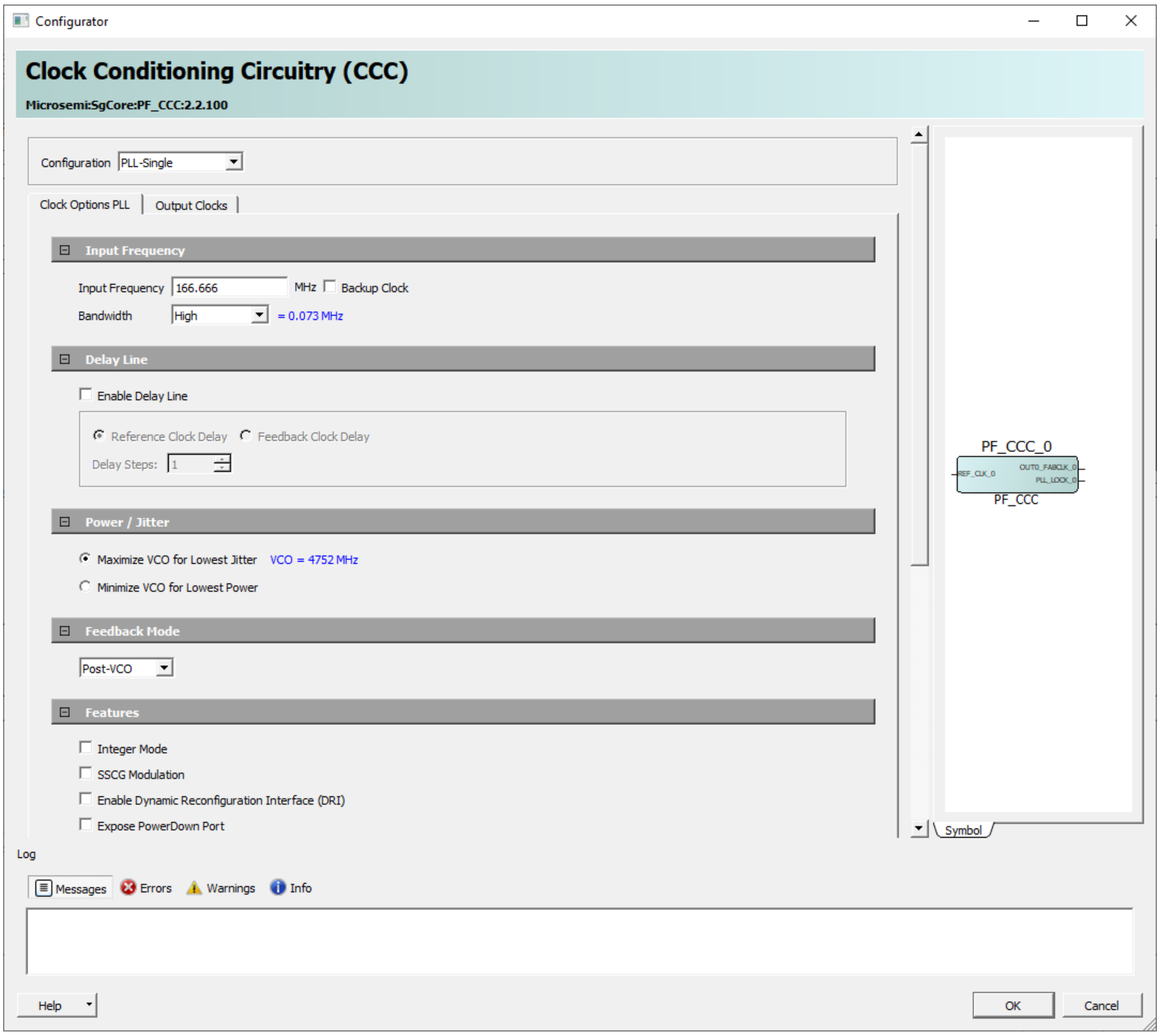
Image Enhancement Configurator

Microsemi:SolutionCore:DisplayEnhancements:2.0.0

g_YCbCr_DATA_BIT_WIDTH:	8
g_B_C_SAT_CONSTANT_WIDTH:	8
g_HUE_CONSTANT_WIDTH:	9
g_SIN_COS_DWIDTH:	10
g_SIN_COS_MEM_DEPTH:	180
testbench:	User
License:	Obfuscated

Figure 13: DisplayEnhancement_0_0 Configuration

3.3.1.8 IP Core PF_CCC_3_0


Configurator

Clock Conditioning Circuitry (CCC)

Microsemi:SgCore:PF_CCC:2.2.100

Configuration: PLL-Single

Clock Options PLL | Output Clocks

Input Frequency

Input Frequency: 166.666 MHz ☐ Backup Clock

Bandwidth: High = 0.073 MHz

Delay Line

☐ Enable Delay Line

[✓ Reference Clock Delay] Feedback Clock Delay

Delay Steps: 1

Power / Jitter

[✓ Maximize VCO for Lowest Jitter] VCO = 4752 MHz

Minimize VCO for Lowest Power

Feedback Mode

Post-VCO

Features

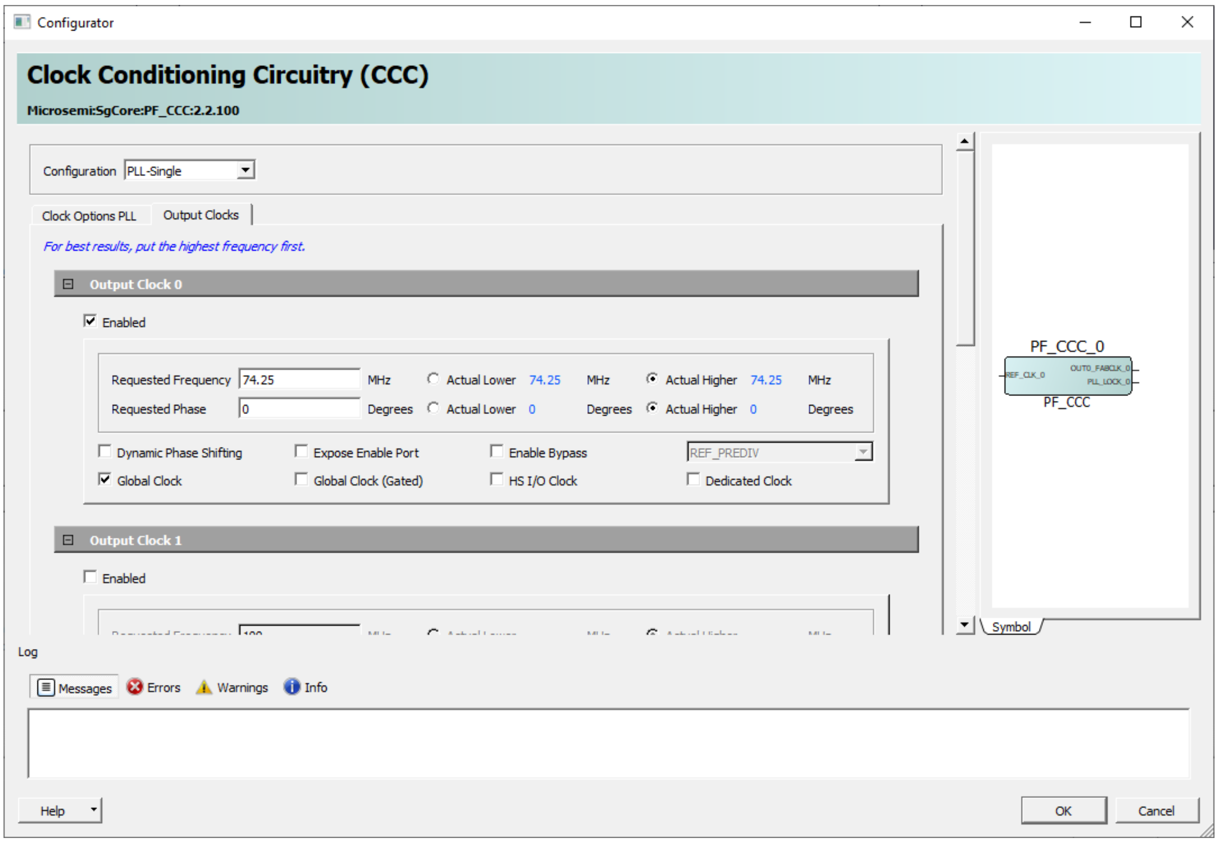
☐ Integer Mode

☐ SSCG Modulation

☐ Enable Dynamic Reconfiguration Interface (DRI)

☐ Expose PowerDown Port

Figure 14: PF_CCC_3_0 Clock Options PLL



Configurator

Clock Conditioning Circuitry (CCC)

Microsemi:SgCore:PF_CCC:2.2.100

Configuration: PLL-Single

Clock Options PLL | Output Clocks

For best results, put the highest frequency first.

Output Clock 0

☑ Enabled

Requested Frequency: 74.25 MHz — ○ Actual Lower 74.25 MHz — ● Actual Higher 74.25 MHz

Requested Phase: 0 Degrees — ○ Actual Lower 0 Degrees — ● Actual Higher 0 Degrees

☐ Dynamic Phase Shifting ☐ Expose Enable Port ☐ Enable Bypass REF_PREDIV

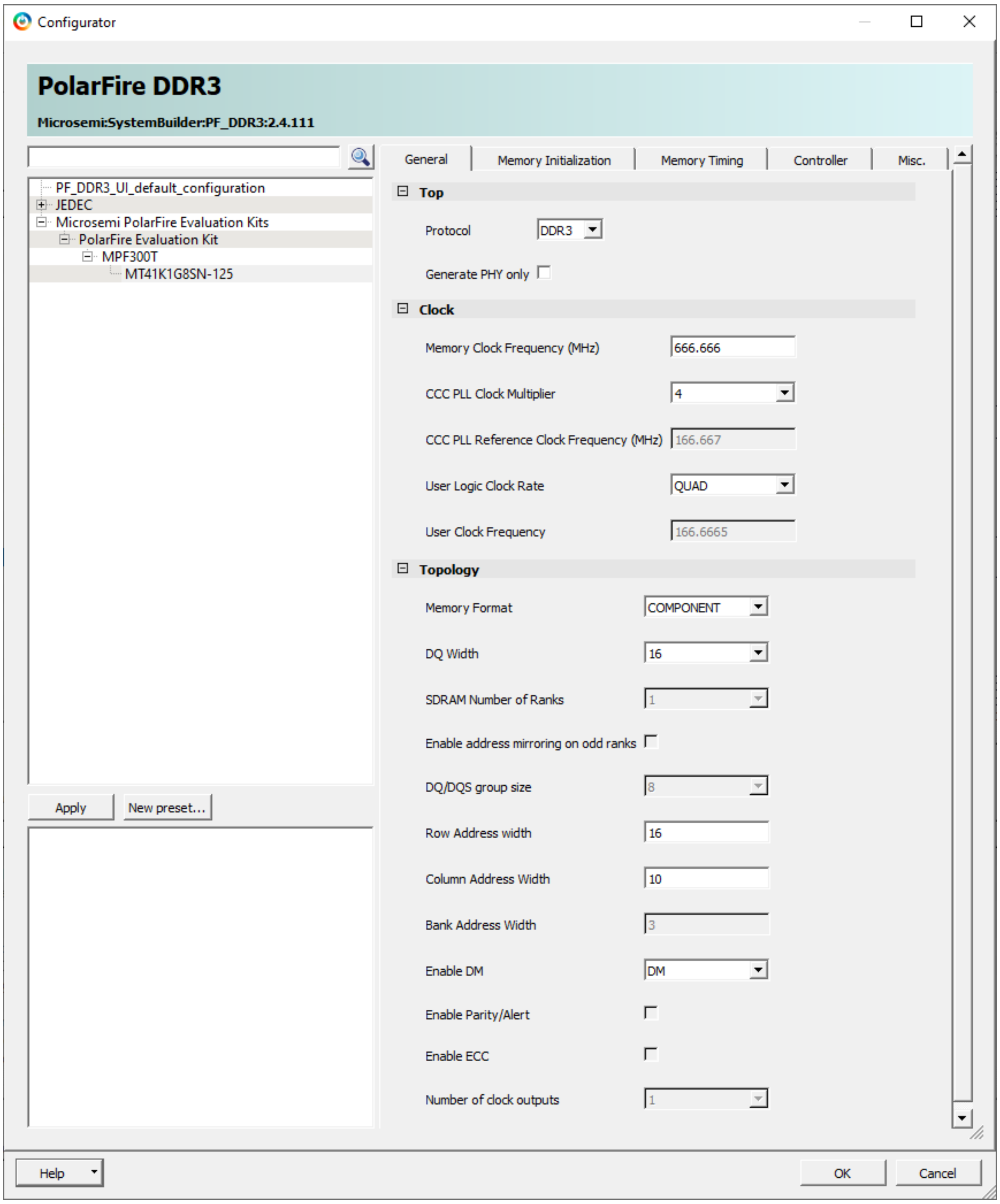
☑ Global Clock ☐ Global Clock (Gated) ☐ HS I/O Clock ☐ Dedicated Clock

Output Clock 1

☐ Enabled

Figure 15: PF_CCC_3_0 Output Clock

3.3.1.9 IP Core PF_DDR_CNTRLR_0_0



Top

Protocol	DDR3
Generate PHY only	☐

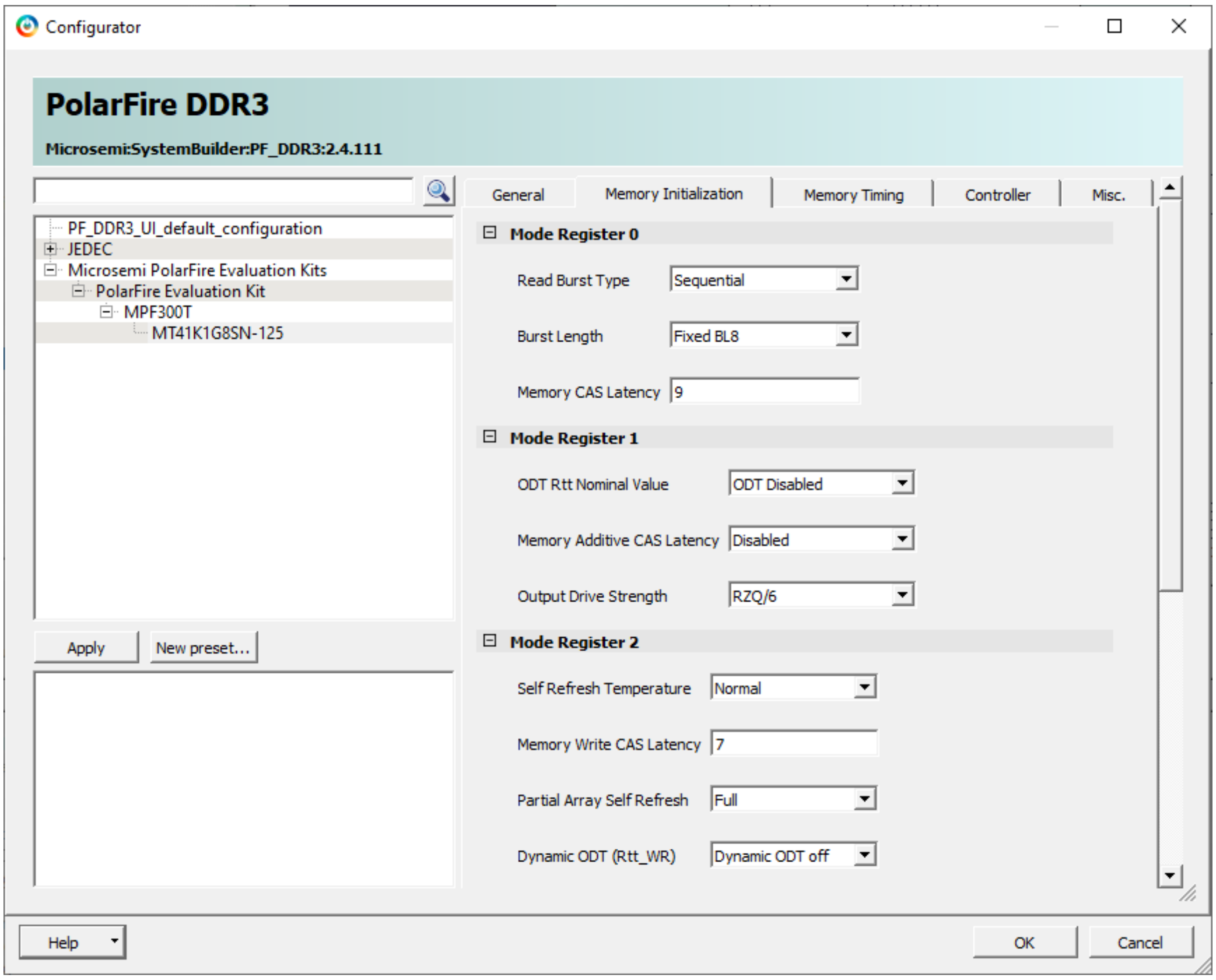
Clock

Memory Clock Frequency (MHz)	666.666
CCC PLL Clock Multiplier	4
CCC PLL Reference Clock Frequency (MHz)	166.667
User Logic Clock Rate	QUAD
User Clock Frequency	166.6665

Topology

Memory Format	COMPONENT
DQ Width	16
SDRAM Number of Ranks	1
Enable address mirroring on odd ranks	☐
DQ/DQS group size	8
Row Address width	16
Column Address Width	10
Bank Address Width	3
Enable DM	DM
Enable Parity/Alert	☐
Enable ECC	☐
Number of clock outputs	1

Figure 16: PF_DDR_CNTRLR_0_0 General



Mode Register 0

Read Burst Type	Sequential
Burst Length	Fixed BL8
Memory CAS Latency	9

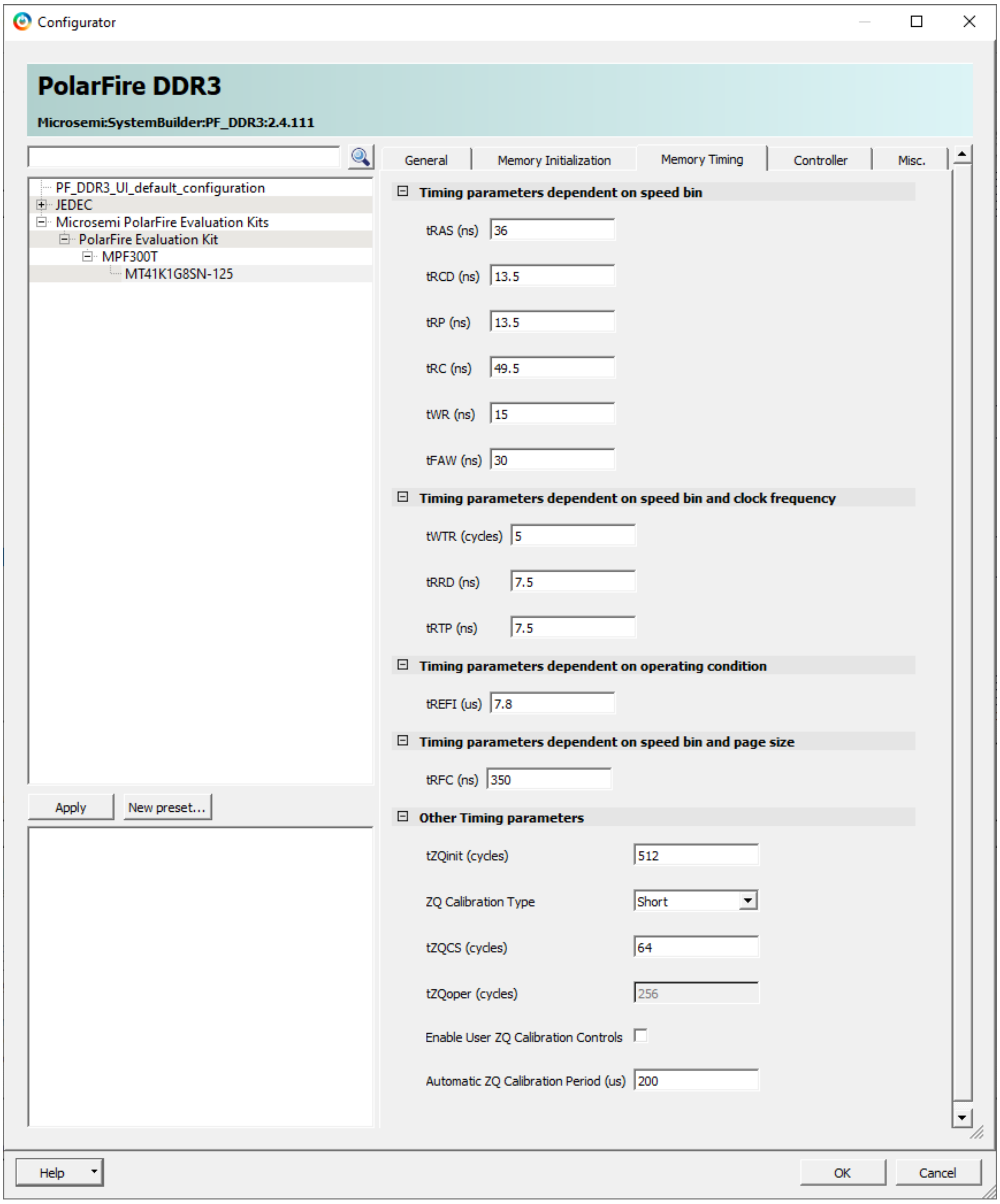
Mode Register 1

ODT Rtt Nominal Value	ODT Disabled
Memory Additive CAS Latency	Disabled
Output Drive Strength	RZQ/6

Mode Register 2

Self Refresh Temperature	Normal
Memory Write CAS Latency	7
Partial Array Self Refresh	Full
Dynamic ODT (Rtt_WR)	Dynamic ODT off

Figure 17: PF_DDR_CNTRLR_0_0 Memory Initialization



PolarFire DDR3

Microsemi:SystemBuilder:PF_DDR3:2.4.111

- PF_DDR3_UI_default_configuration
- JEDEC
- Microsemi PolarFire Evaluation Kits
  - PolarFire Evaluation Kit
    - MPF300T
      - MT41K1G8SN-125

Timing parameters dependent on speed bin

tRAS (ns)	36
tRCD (ns)	13.5
tRP (ns)	13.5
tRC (ns)	49.5
tWR (ns)	15
tFAW (ns)	30

Timing parameters dependent on speed bin and clock frequency

tWTR (cycles)	5
tRRD (ns)	7.5
tRTP (ns)	7.5

Timing parameters dependent on operating condition

tREFI (us)	7.8

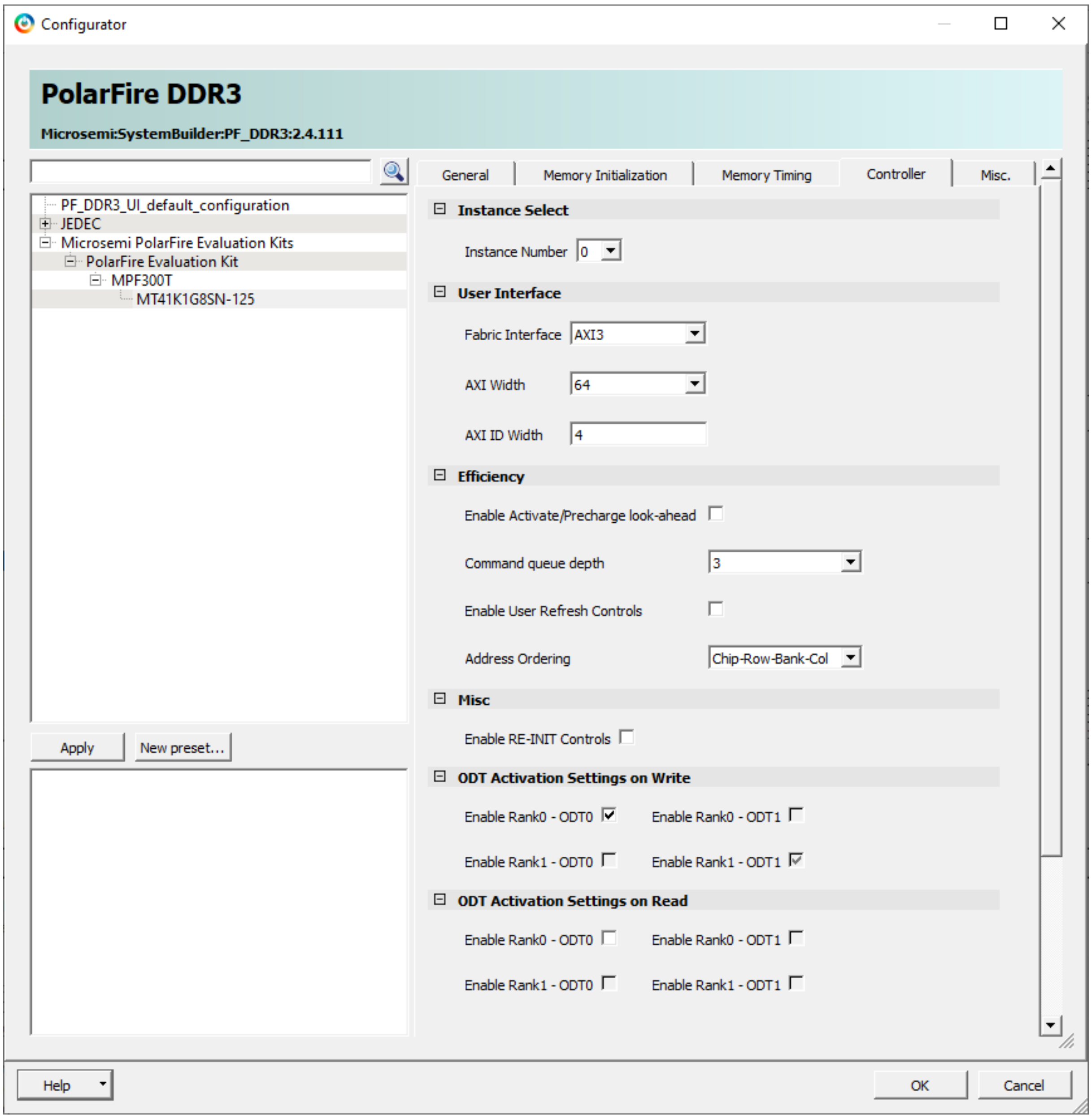
Timing parameters dependent on speed bin and page size

tRFC (ns)	350

Other Timing parameters

tZQinit (cycles)	512
ZQ Calibration Type	Short
tZQCS (cycles)	64
tZQoper (cycles)	256
Enable User ZQ Calibration Controls	☐
Automatic ZQ Calibration Period (us)	200

Figure 18: PF_DDR_CNTRLR_0_0 Memory Timing


Configurator

PolarFire DDR3

Microsemi:SystemBuilder:PF_DDR3:2.4.111

- PF_DDR3_UI_default_configuration
- JEDEC
- Microsemi PolarFire Evaluation Kits
  - PolarFire Evaluation Kit
    - MPF300T
      - MT41K1G8SN-125

Instance Select

Instance Number: 0

User Interface

Fabric Interface: AXI3

AXI Width: 64

AXI ID Width: 4

Efficiency

Enable Activate/Precharge look-ahead ☐

Command queue depth: 3

Enable User Refresh Controls ☐

Address Ordering: Chip-Row-Bank-Col

Misc

Enable RE-INIT Controls ☐

ODT Activation Settings on Write

Enable Rank0 - ODT0 ☑ Enable Rank0 - ODT1 ☐

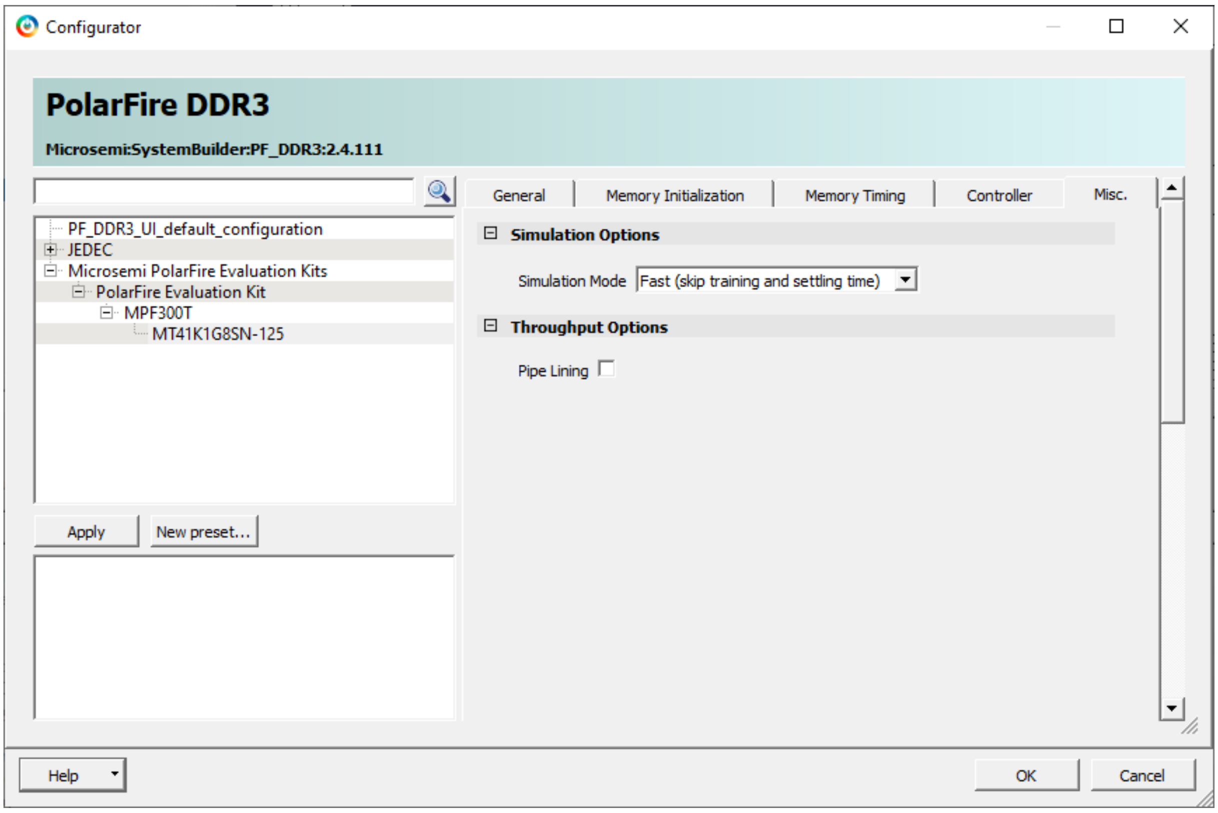
Enable Rank1 - ODT0 ☐ Enable Rank1 - ODT1 ☑

ODT Activation Settings on Read

Enable Rank0 - ODT0 ☐ Enable Rank0 - ODT1 ☐

Enable Rank1 - ODT0 ☐ Enable Rank1 - ODT1 ☐

Figure 19: PF_DDR_CNTRLR_0_0 Controller


Configurator

PolarFire DDR3

Microsemi:SystemBuilder:PF_DDR3:2.4.111

- PF_DDR3_UI_default_configuration
- JEDEC
- Microsemi PolarFire Evaluation Kits
  - PolarFire Evaluation Kit
    - MPF300T
      - MT41K1G8SN-125

Simulation Options

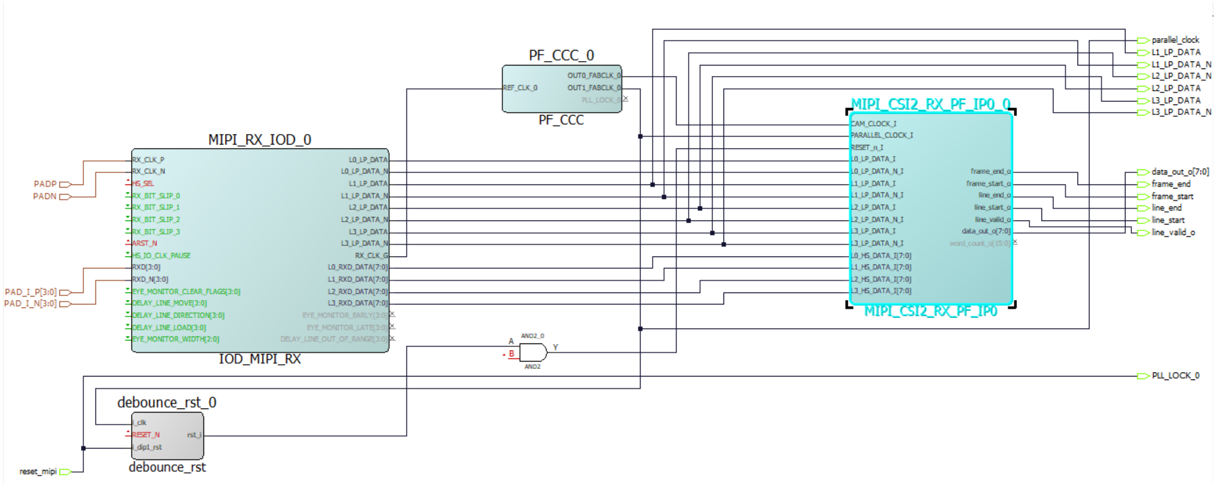
Simulation Mode: Fast (skip training and settling time)

Throughput Options

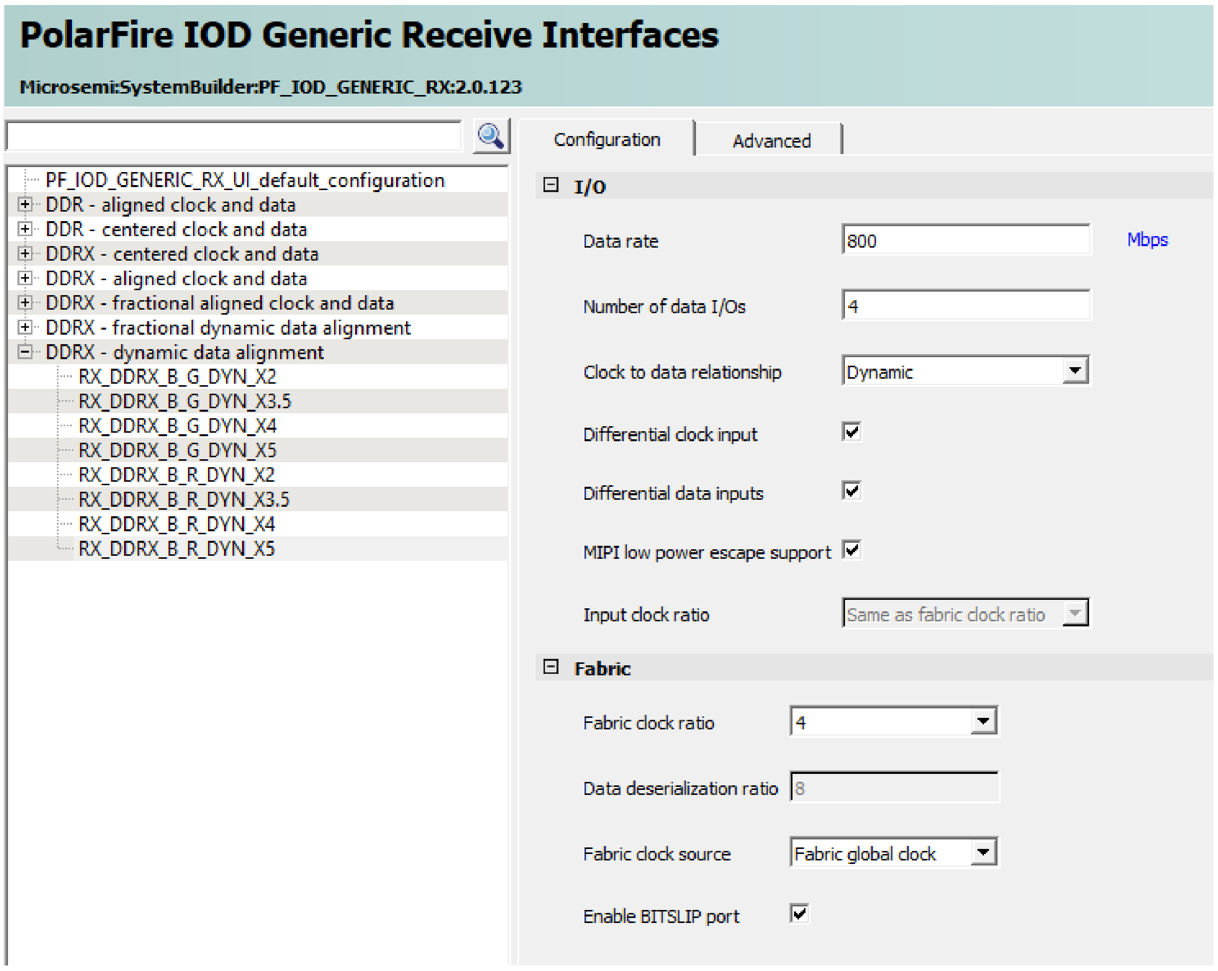
Pipe Lining ☐

Figure 20: PF_DDR_CNTRLR_0_0 Misc.

3.3.2 Smart Design cam_ar0331_mipi



3.3.2.1 IP Core MIPI_RX_IOD_0


PolarFire IOD Generic Receive Interfaces

Microsemi:SystemBuilder:PF_IOD_GENERIC_RX:2.0.123

PF_IOD_GENERIC_RX_UI_default_configuration
DDR - aligned clock and data
DDR - centered clock and data
DDRX - centered clock and data
DDRX - aligned clock and data
DDRX - fractional aligned clock and data
DDRX - fractional dynamic data alignment
DDRX - dynamic data alignment
RX_DDRX_B_G_DYN_X2
RX_DDRX_B_G_DYN_X3.5
RX_DDRX_B_G_DYN_X4
RX_DDRX_B_G_DYN_X5
RX_DDRX_B_R_DYN_X2
RX_DDRX_B_R_DYN_X3.5
RX_DDRX_B_R_DYN_X4
RX_DDRX_B_R_DYN_X5
Configuration
Advanced

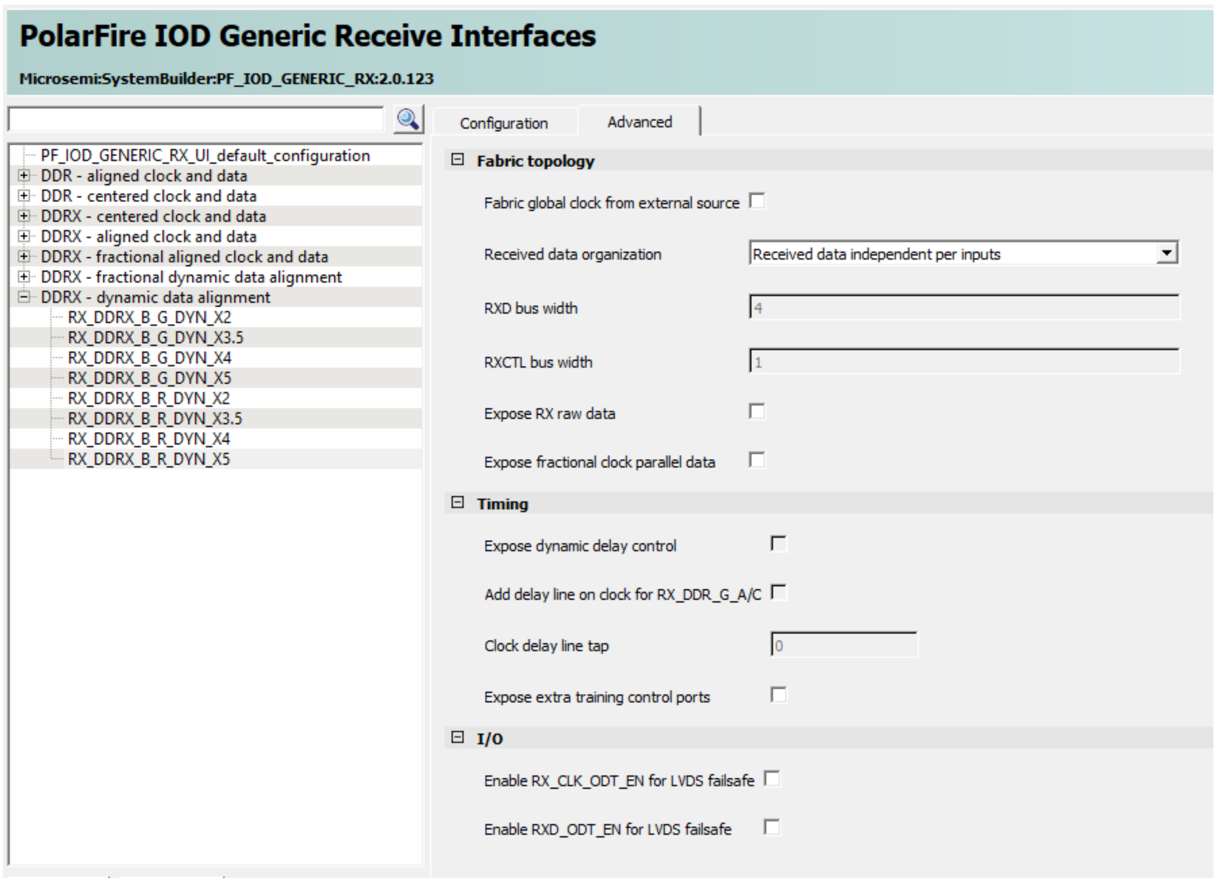
I/O

Data rate	800 Mbps
Number of data I/Os	4
Clock to data relationship	Dynamic
Differential clock input	✓
Differential data inputs	✓
MIPI low power escape support	✓
Input clock ratio	Same as fabric clock ratio

Fabric

Fabric clock ratio	4
Data deserialization ratio	8
Fabric clock source	Fabric global clock
Enable BITSLIP port	✓

Figure 21: MIPI_RX_IOD_0 Configuration



PolarFire IOD Generic Receive Interfaces

Microsemi:SystemBuilder:PF_IOD_GENERIC_RX:2.0.123

- PF_IOD_GENERIC_RX_UI_default_configuration
- DDR - aligned clock and data
- DDR - centered clock and data
- DDRX - centered clock and data
- DDRX - aligned clock and data
- DDRX - fractional aligned clock and data
- DDRX - fractional dynamic data alignment
- DDRX - dynamic data alignment
  - RX_DDRX_B_G_DYN_X2
  - RX_DDRX_B_G_DYN_X3.5
  - RX_DDRX_B_G_DYN_X4
  - RX_DDRX_B_G_DYN_X5
  - RX_DDRX_B_R_DYN_X2
  - RX_DDRX_B_R_DYN_X3.5
  - RX_DDRX_B_R_DYN_X4
  - RX_DDRX_B_R_DYN_X5

Configuration | Advanced

Fabric topology

Fabric global clock from external source	☐
Received data organization	Received data independent per inputs
RXD bus width	4
RXCTL bus width	1
Expose RX raw data	☐
Expose fractional clock parallel data	☐

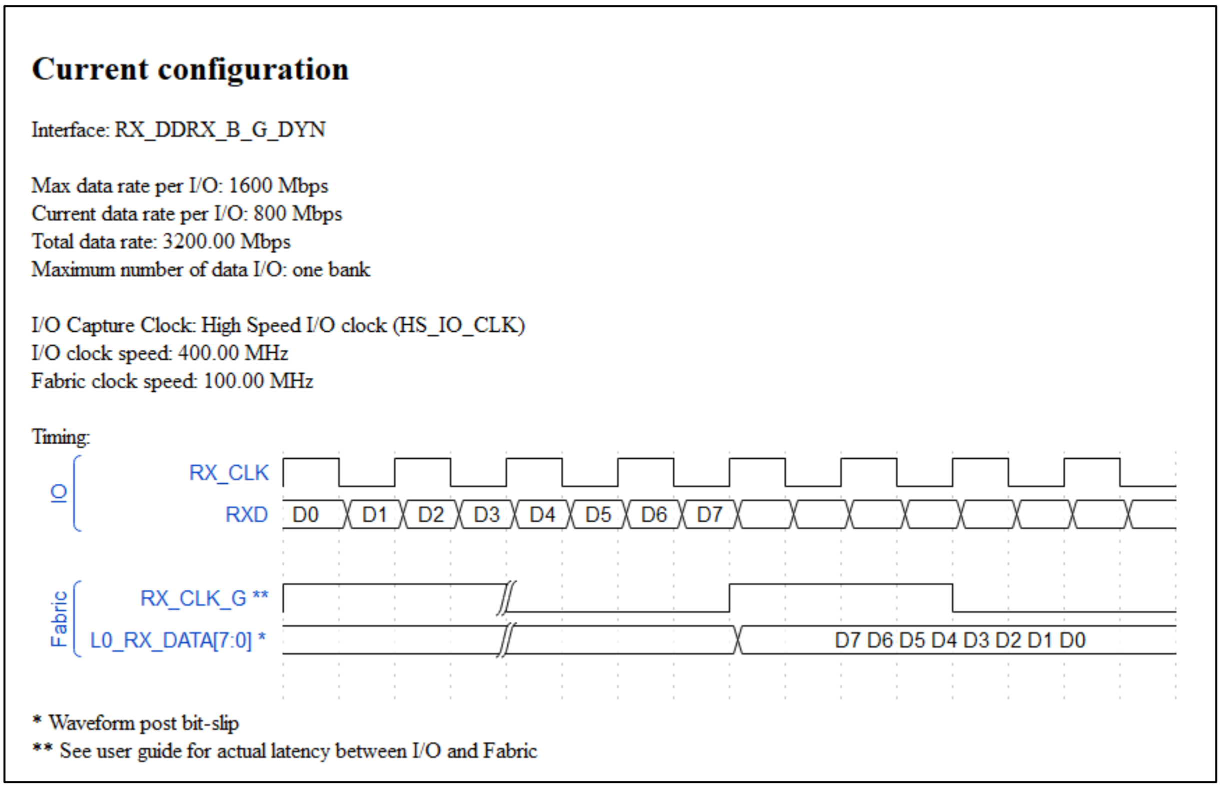
Timing

Expose dynamic delay control	☐
Add delay line on clock for RX_DDR_G_A/C	☐
Clock delay line tap	0
Expose extra training control ports	☐

I/O

Enable RX_CLK_ODT_EN for LVDS failsafe	☐
Enable RXD_ODT_EN for LVDS failsafe	☐

Figure 22: MIPI_RX_IOD_0 Advanced



Current configuration

Interface: RX_DDRX_B_G_DYN

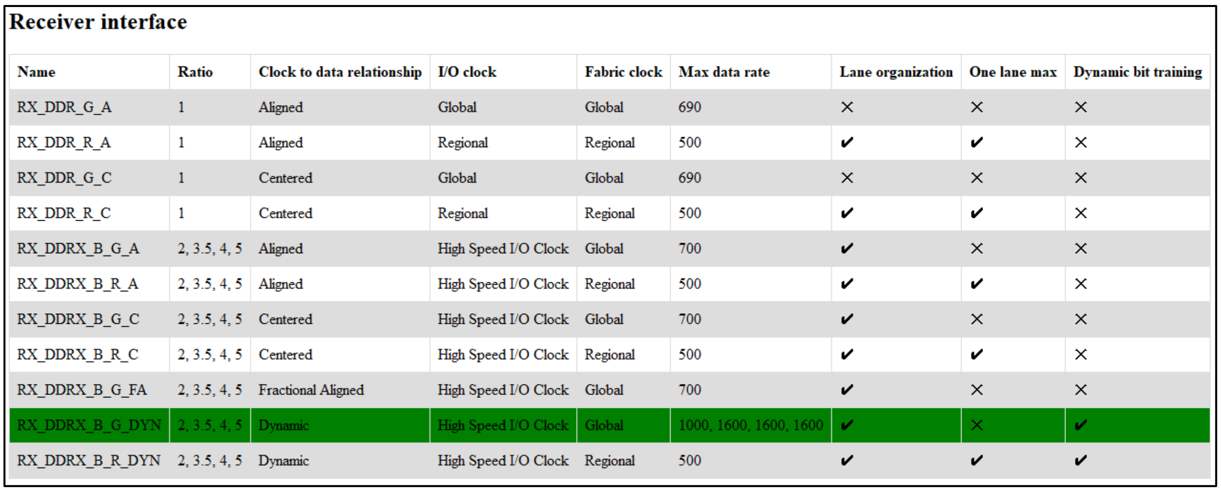
Max data rate per I/O: 1600 Mbps
Current data rate per I/O: 800 Mbps
Total data rate: 3200.00 Mbps
Maximum number of data I/O: one bank

I/O Capture Clock: High Speed I/O clock (HS_IO_CLK)
I/O clock speed: 400.00 MHz
Fabric clock speed: 100.00 MHz

Timing:

* Waveform post bit-slip
** See user guide for actual latency between I/O and Fabric

Figure 23: MIPI_RX_IOD_0 Current configuration

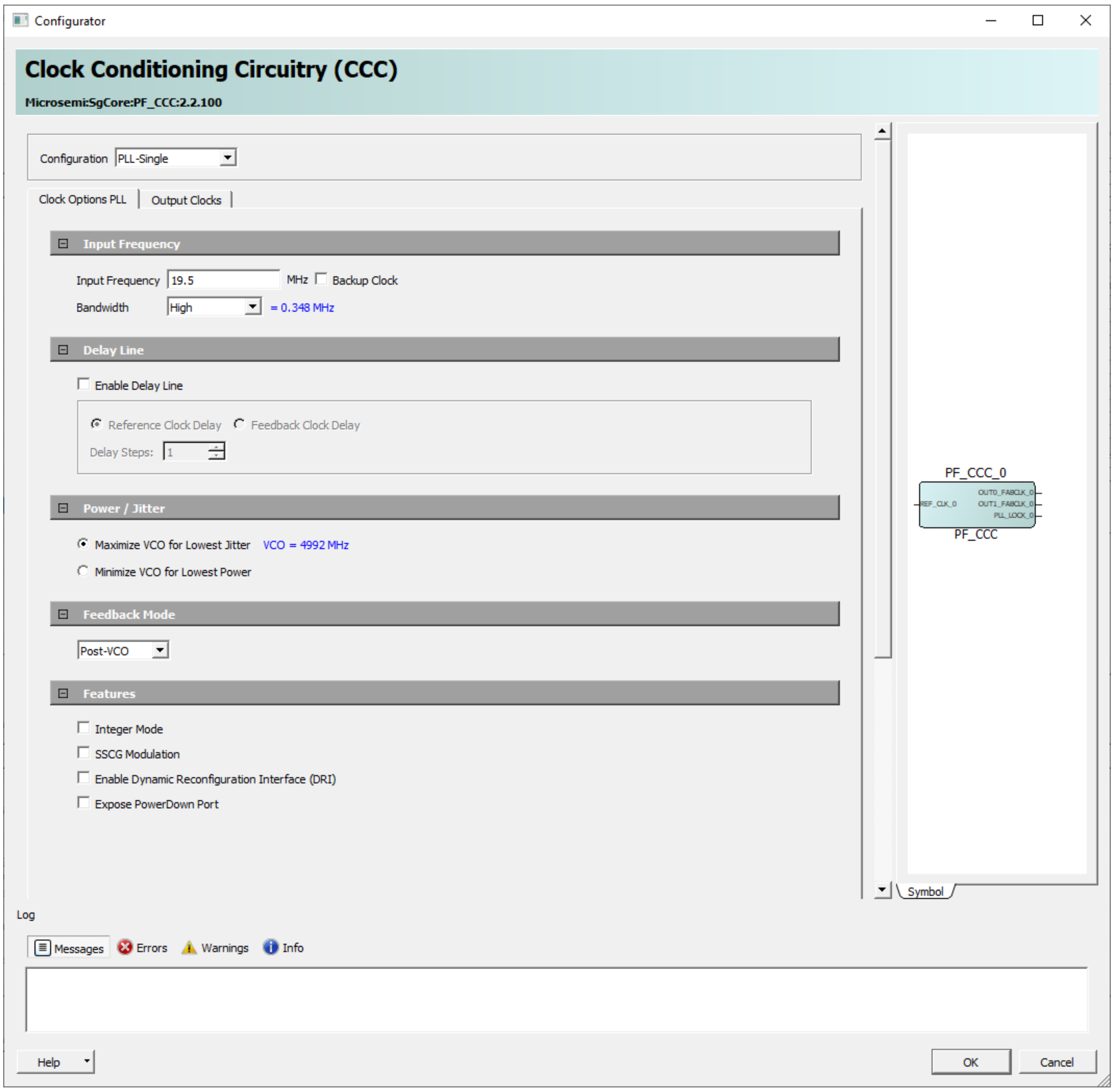


Receiver interface

Name	Ratio	Clock to data relationship	I/O clock	Fabric clock	Max data rate	Lane organization	One lane max	Dynamic bit training
RX_DDR_G_A	1	Aligned	Global	Global	690	×	×	×
RX_DDR_R_A	1	Aligned	Regional	Regional	500	✔	✔	×
RX_DDR_G_C	1	Centered	Global	Global	690	×	×	×
RX_DDR_R_C	1	Centered	Regional	Regional	500	✔	✔	×
RX_DDRX_B_G_A	2, 3.5, 4, 5	Aligned	High Speed I/O Clock	Global	700	✔	×	×
RX_DDRX_B_R_A	2, 3.5, 4, 5	Aligned	High Speed I/O Clock	Regional	500	✔	✔	×
RX_DDRX_B_G_C	2, 3.5, 4, 5	Centered	High Speed I/O Clock	Global	700	✔	×	×
RX_DDRX_B_R_C	2, 3.5, 4, 5	Centered	High Speed I/O Clock	Regional	500	✔	✔	×
RX_DDRX_B_G_FA	2, 3.5, 4, 5	Fractional Aligned	High Speed I/O Clock	Global	700	✔	×	×
RX_DDRX_B_G_DYN	2, 3.5, 4, 5	Dynamic	High Speed I/O Clock	Global	1000, 1600, 1600, 1600	✔	×	✔
RX_DDRX_B_R_DYN	2, 3.5, 4, 5	Dynamic	High Speed I/O Clock	Regional	500	✔	✔	✔

Figure 24: MIPI_RX_IOD_0 Receiver interface

3.3.2.2 IP Core PF_CCC_0


Configurator

Clock Conditioning Circuitry (CCC)

Microsemi:SgCore:PF_CCC:2.2.100

Configuration: PLL-Single

Clock Options PLL | Output Clocks

Input Frequency

Input Frequency: 19.5 MHz ☐ Backup Clock

Bandwidth: High = 0.348 MHz

Delay Line

☐ Enable Delay Line

[✓ Reference Clock Delay] Feedback Clock Delay

Delay Steps: 1

Power / Jitter

[✓ Maximize VCO for Lowest Jitter] VCO = 4992 MHz

Minimize VCO for Lowest Power

Feedback Mode

Post-VCO

Features

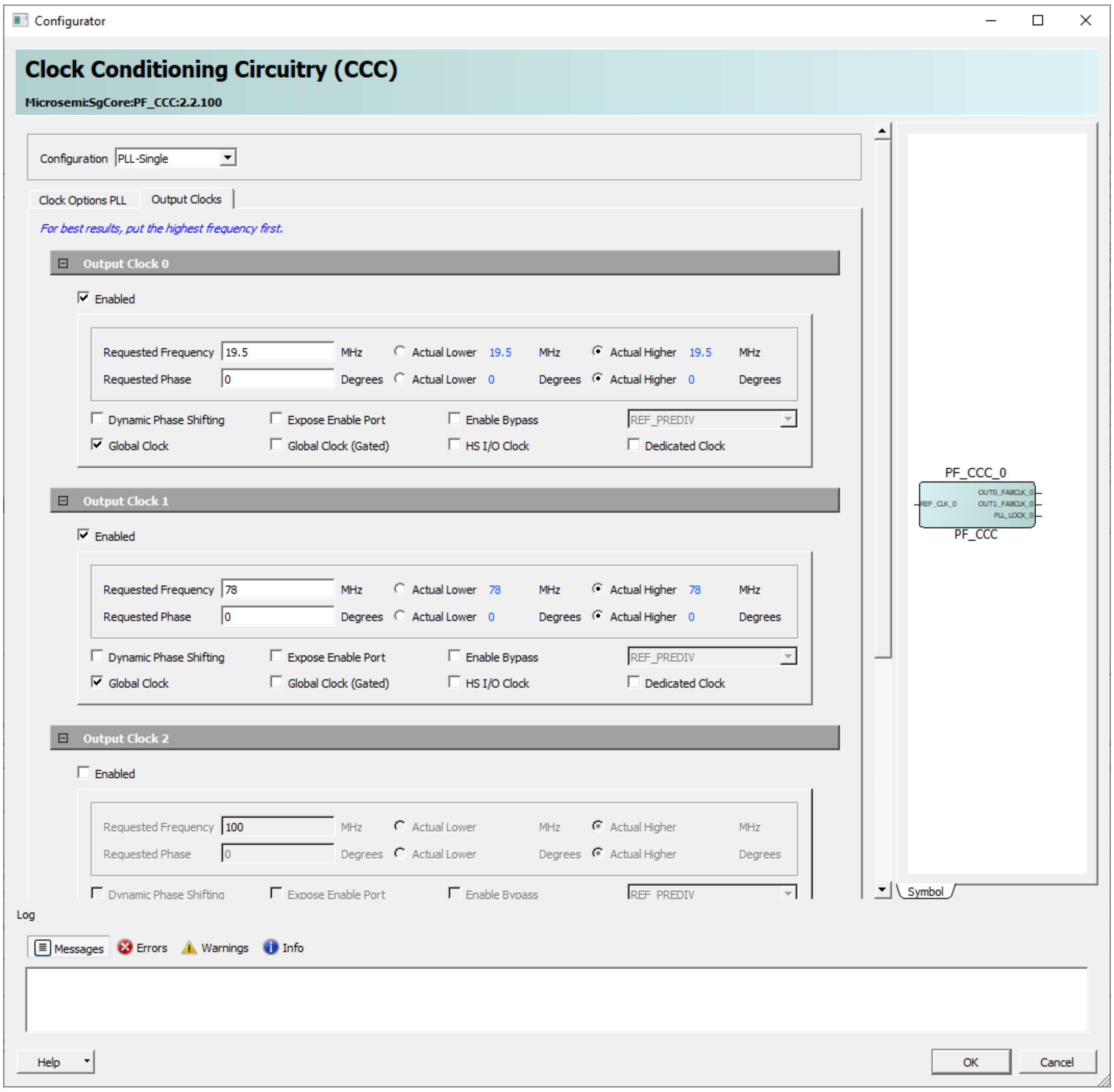
☐ Integer Mode

☐ SSCG Modulation

☐ Enable Dynamic Reconfiguration Interface (DRI)

☐ Expose PowerDown Port

Figure 25: PF_CCC_0 Clock Options PLL


Configurator

Clock Conditioning Circuitry (CCC)
Microsemi:SgCore:PF_CCC:2.2.100

Configuration: PLL-Single

Clock Options PLL | Output Clocks

For best results, put the highest frequency first.

Output Clock 0

[✓] Enabled

Requested Frequency: 19.5 MHz — ( ) Actual Lower 19.5 MHz — (●) Actual Higher 19.5 MHz
Requested Phase: 0 Degrees — ( ) Actual Lower 0 Degrees — (●) Actual Higher 0 Degrees

[ ] Dynamic Phase Shifting — [ ] Expose Enable Port — [ ] Enable Bypass — REF_PREDIV
[✓] Global Clock — [ ] Global Clock (Gated) — [ ] HS I/O Clock — [ ] Dedicated Clock

Output Clock 1

[✓] Enabled

Requested Frequency: 78 MHz — ( ) Actual Lower 78 MHz — (●) Actual Higher 78 MHz
Requested Phase: 0 Degrees — ( ) Actual Lower 0 Degrees — (●) Actual Higher 0 Degrees

[ ] Dynamic Phase Shifting — [ ] Expose Enable Port — [ ] Enable Bypass — REF_PREDIV
[✓] Global Clock — [ ] Global Clock (Gated) — [ ] HS I/O Clock — [ ] Dedicated Clock

Output Clock 2

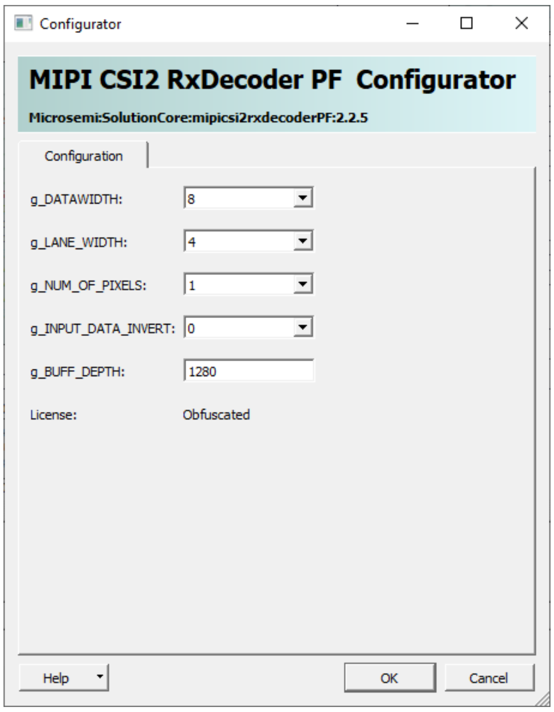
[ ] Enabled

Requested Frequency: 100 MHz — ( ) Actual Lower MHz — (●) Actual Higher MHz
Requested Phase: 0 Degrees — ( ) Actual Lower Degrees — (●) Actual Higher Degrees

[ ] Dynamic Phase Shifting — [ ] Expose Enable Port — [ ] Enable Bypass — REF_PREDIV

Figure 26: PF_CCC_0 Output Clocks

3.3.2.3 IP Core MIPI_CSI2_RX_PF_IP0_0



MIPI CSI2 RxDecoder PF Configurator
Microsemi:SolutionCore:mipicsi2rxdecoderPF:2.2.5

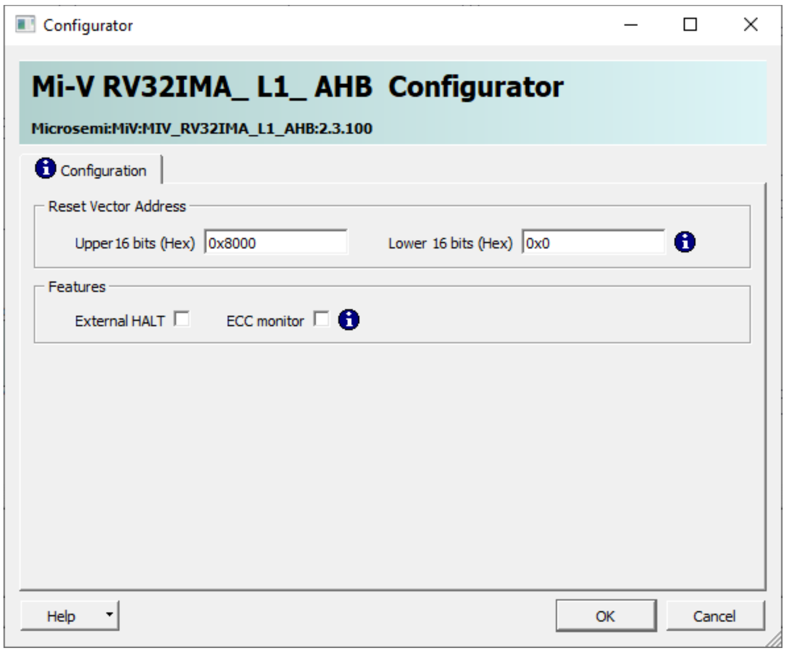
Configuration

g_DATAWIDTH:	8
g_LANE_WIDTH:	4
g_NUM_OF_PIXELS:	1
g_INPUT_DATA_INVERT:	0
g_BUFF_DEPTH:	1280
License:	Obfuscated

Figure 27: MIPI_CSI2_RX_PF_IP0_0 Configuration

3.3.3 Smart Design PROC_SUBSYSTEM

3.3.3.1 IP Core Mi_V_Processor_0_0



Mi-V RV32IMA_ L1_ AHB Configurator
Microsemi:MiV:MIV_RV32IMA_L1_AHB:2.3.100

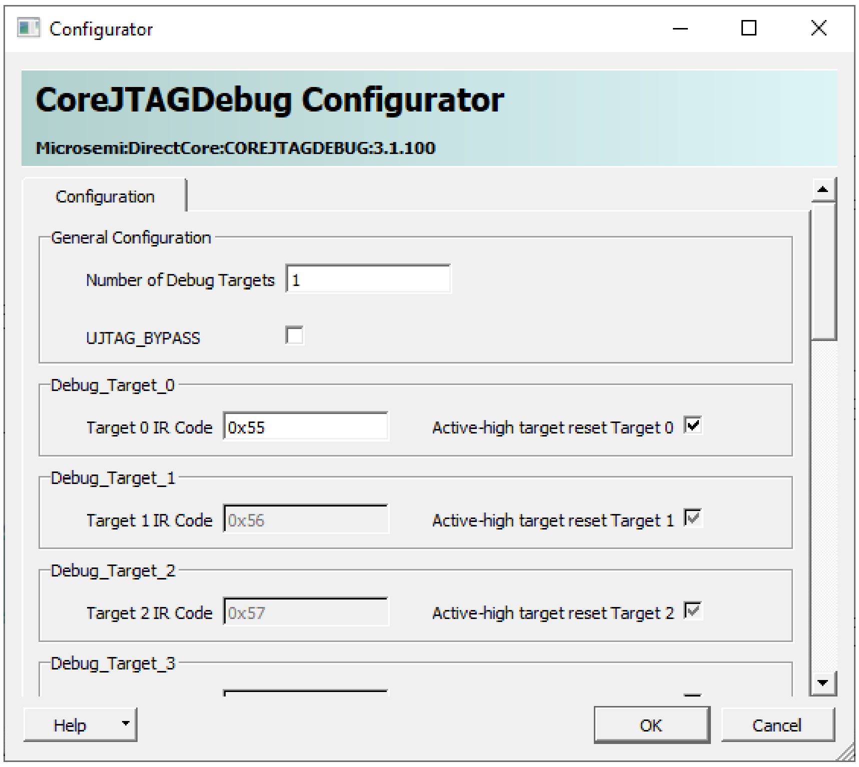
Configuration

Reset Vector Address
Upper 16 bits (Hex) 0x8000 Lower 16 bits (Hex) 0x0

Features
External HALT ☐ ECC monitor ☐

Figure 28: RV32IMA_L1_AHB Configuration

3.3.3.2 IP Core COREJTAGDEBUG_0


Configurator
CoreJTAGDebug Configurator
Microsemi:DirectCore:COREJTAGDEBUG:3.1.100
Configuration
Help
OK
Cancel

General Configuration

Number of Debug Targets: 1

UJTAG_BYPASS: ☐

Debug_Target_0

Target 0 IR Code: 0x55 — Active-high target reset Target 0: ✓

Debug_Target_1

Target 1 IR Code: 0x56 — Active-high target reset Target 1: ✓

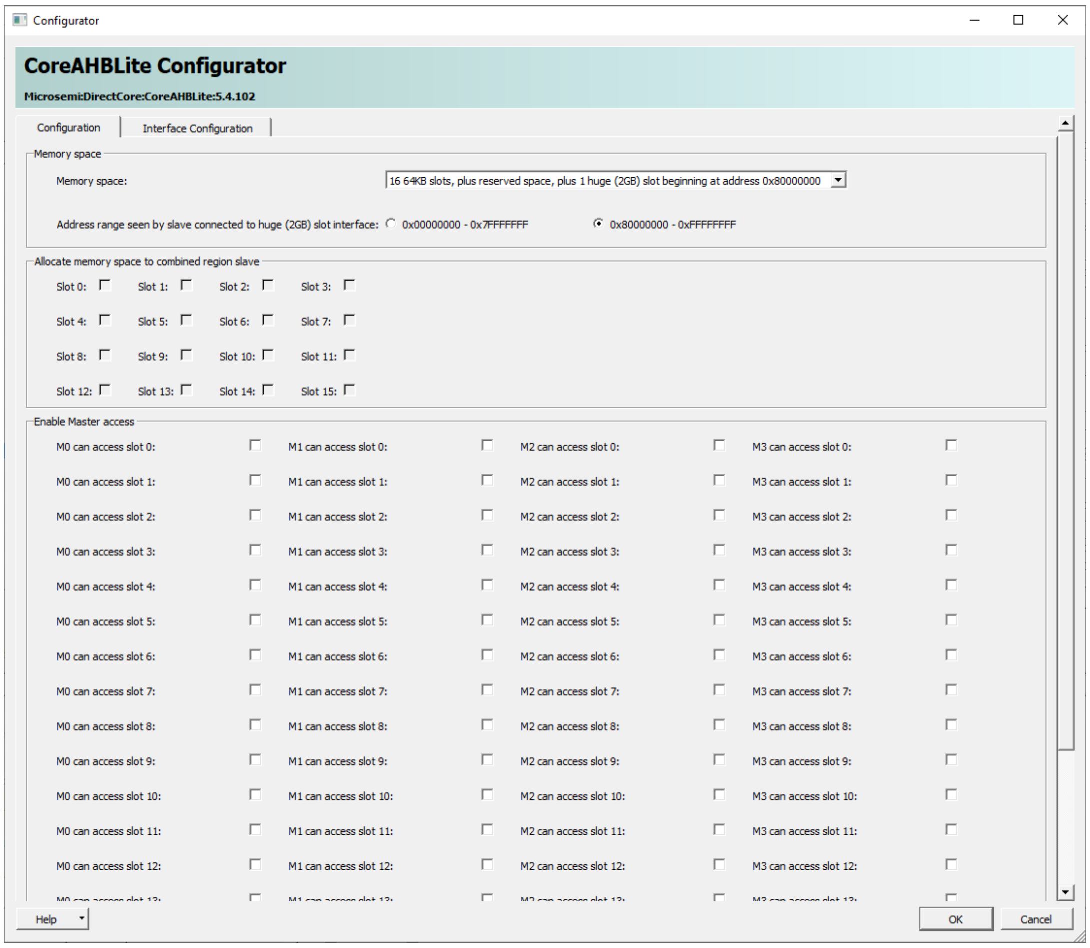
Debug_Target_2

Target 2 IR Code: 0x57 — Active-high target reset Target 2: ✓

Debug_Target_3

Figure 29: CoreJTAGDebug Configuration

3.3.3.3 IP Core CoreAHBLite_1_0



Configurator

CoreAHBLite Configurator

Microsemi:DirectCore:CoreAHBLite:5.4.102

Configuration | Interface Configuration

Memory space

Memory space: 16 64KB slots, plus reserved space, plus 1 huge (2GB) slot beginning at address 0x80000000

Address range seen by slave connected to huge (2GB) slot interface: 0x00000000 - 0x7FFFFFFF [✓ 0x80000000 - 0xFFFFFFFF]

Allocate memory space to combined region slave

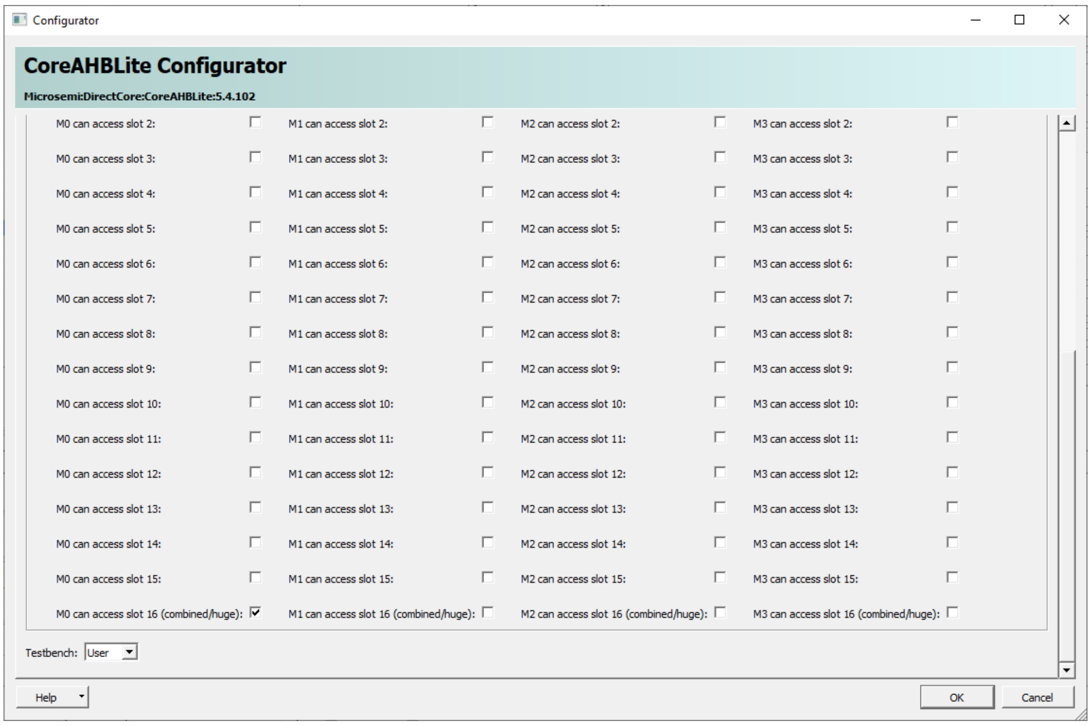
Slot 0: ☐	Slot 1: ☐	Slot 2: ☐	Slot 3: ☐
Slot 4: ☐	Slot 5: ☐	Slot 6: ☐	Slot 7: ☐
Slot 8: ☐	Slot 9: ☐	Slot 10: ☐	Slot 11: ☐
Slot 12: ☐	Slot 13: ☐	Slot 14: ☐	Slot 15: ☐

Enable Master access

M0 can access slot 0:	☐	M1 can access slot 0:	☐	M2 can access slot 0:	☐	M3 can access slot 0:	☐
M0 can access slot 1:	☐	M1 can access slot 1:	☐	M2 can access slot 1:	☐	M3 can access slot 1:	☐
M0 can access slot 2:	☐	M1 can access slot 2:	☐	M2 can access slot 2:	☐	M3 can access slot 2:	☐
M0 can access slot 3:	☐	M1 can access slot 3:	☐	M2 can access slot 3:	☐	M3 can access slot 3:	☐
M0 can access slot 4:	☐	M1 can access slot 4:	☐	M2 can access slot 4:	☐	M3 can access slot 4:	☐
M0 can access slot 5:	☐	M1 can access slot 5:	☐	M2 can access slot 5:	☐	M3 can access slot 5:	☐
M0 can access slot 6:	☐	M1 can access slot 6:	☐	M2 can access slot 6:	☐	M3 can access slot 6:	☐
M0 can access slot 7:	☐	M1 can access slot 7:	☐	M2 can access slot 7:	☐	M3 can access slot 7:	☐
M0 can access slot 8:	☐	M1 can access slot 8:	☐	M2 can access slot 8:	☐	M3 can access slot 8:	☐
M0 can access slot 9:	☐	M1 can access slot 9:	☐	M2 can access slot 9:	☐	M3 can access slot 9:	☐
M0 can access slot 10:	☐	M1 can access slot 10:	☐	M2 can access slot 10:	☐	M3 can access slot 10:	☐
M0 can access slot 11:	☐	M1 can access slot 11:	☐	M2 can access slot 11:	☐	M3 can access slot 11:	☐
M0 can access slot 12:	☐	M1 can access slot 12:	☐	M2 can access slot 12:	☐	M3 can access slot 12:	☐

Help | OK | Cancel

Figure 30: CoreAHBLite_1_0 Configuration



Configurator

CoreAHBLite Configurator

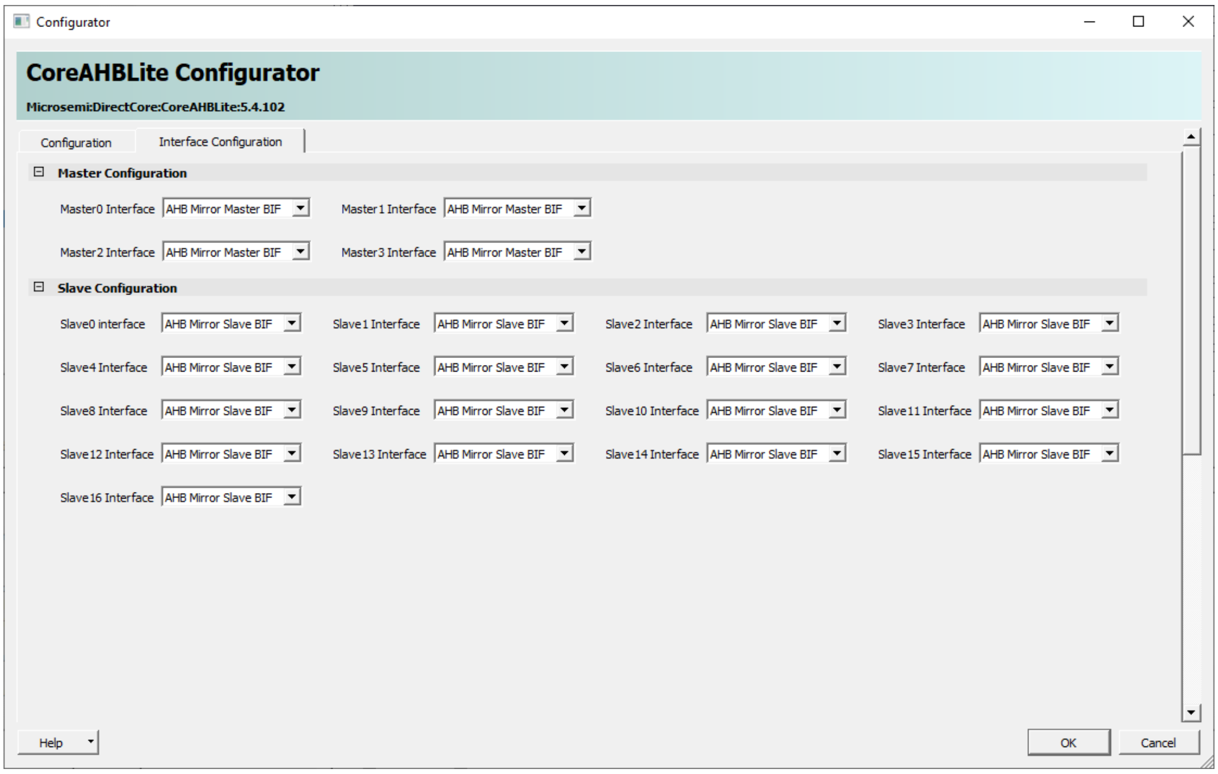
Microsemi:DirectCore:CoreAHBLite:5.4.102

M0 can access slot 2:	☐	M1 can access slot 2:	☐	M2 can access slot 2:	☐	M3 can access slot 2:	☐
M0 can access slot 3:	☐	M1 can access slot 3:	☐	M2 can access slot 3:	☐	M3 can access slot 3:	☐
M0 can access slot 4:	☐	M1 can access slot 4:	☐	M2 can access slot 4:	☐	M3 can access slot 4:	☐
M0 can access slot 5:	☐	M1 can access slot 5:	☐	M2 can access slot 5:	☐	M3 can access slot 5:	☐
M0 can access slot 6:	☐	M1 can access slot 6:	☐	M2 can access slot 6:	☐	M3 can access slot 6:	☐
M0 can access slot 7:	☐	M1 can access slot 7:	☐	M2 can access slot 7:	☐	M3 can access slot 7:	☐
M0 can access slot 8:	☐	M1 can access slot 8:	☐	M2 can access slot 8:	☐	M3 can access slot 8:	☐
M0 can access slot 9:	☐	M1 can access slot 9:	☐	M2 can access slot 9:	☐	M3 can access slot 9:	☐
M0 can access slot 10:	☐	M1 can access slot 10:	☐	M2 can access slot 10:	☐	M3 can access slot 10:	☐
M0 can access slot 11:	☐	M1 can access slot 11:	☐	M2 can access slot 11:	☐	M3 can access slot 11:	☐
M0 can access slot 12:	☐	M1 can access slot 12:	☐	M2 can access slot 12:	☐	M3 can access slot 12:	☐
M0 can access slot 13:	☐	M1 can access slot 13:	☐	M2 can access slot 13:	☐	M3 can access slot 13:	☐
M0 can access slot 14:	☐	M1 can access slot 14:	☐	M2 can access slot 14:	☐	M3 can access slot 14:	☐
M0 can access slot 15:	☐	M1 can access slot 15:	☐	M2 can access slot 15:	☐	M3 can access slot 15:	☐
M0 can access slot 16 (combined/huge):	✓	M1 can access slot 16 (combined/huge):	☐	M2 can access slot 16 (combined/huge):	☐	M3 can access slot 16 (combined/huge):	☐

Testbench: User

Help | OK | Cancel

Figure 31: CoreAHBLite_1_0 Configuration cont. ...



Configurator

CoreAHBLite Configurator

Microsemi:DirectCore:CoreAHBLite:5.4.102

Configuration | Interface Configuration

Master Configuration

Master0 Interface	AHB Mirror Master BIF	Master1 Interface	AHB Mirror Master BIF
Master2 Interface	AHB Mirror Master BIF	Master3 Interface	AHB Mirror Master BIF

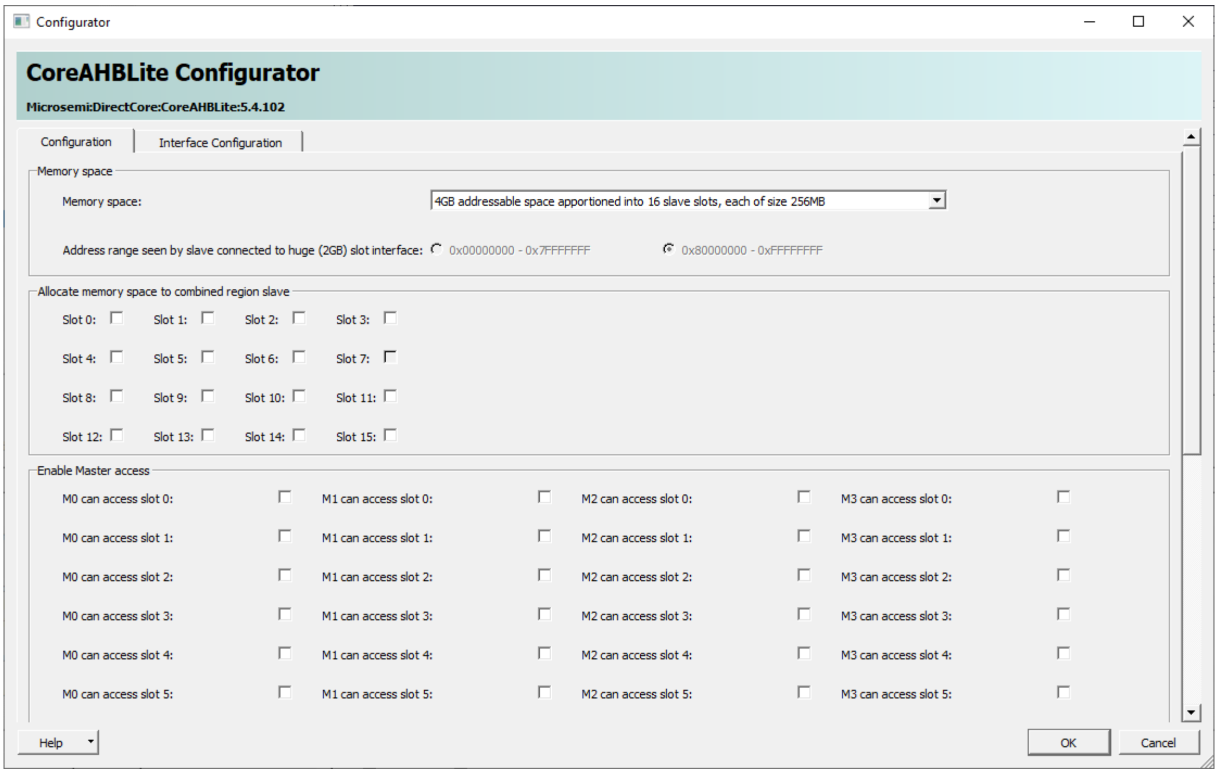
Slave Configuration

Slave0 interface	AHB Mirror Slave BIF	Slave1 Interface	AHB Mirror Slave BIF	Slave2 Interface	AHB Mirror Slave BIF	Slave3 Interface	AHB Mirror Slave BIF
Slave4 Interface	AHB Mirror Slave BIF	Slave5 Interface	AHB Mirror Slave BIF	Slave6 Interface	AHB Mirror Slave BIF	Slave7 Interface	AHB Mirror Slave BIF
Slave8 Interface	AHB Mirror Slave BIF	Slave9 Interface	AHB Mirror Slave BIF	Slave10 Interface	AHB Mirror Slave BIF	Slave11 Interface	AHB Mirror Slave BIF
Slave12 Interface	AHB Mirror Slave BIF	Slave13 Interface	AHB Mirror Slave BIF	Slave14 Interface	AHB Mirror Slave BIF	Slave15 Interface	AHB Mirror Slave BIF
Slave16 Interface	AHB Mirror Slave BIF						

Help | OK | Cancel

Figure 32: CoreAHBLite_1_0 Interface Configuration

3.3.3.4 IP Core CoreAHBLite_0



Configurator

CoreAHBLite Configurator

Microsemi:DirectCore:CoreAHBLite:5.4.102

Configuration | Interface Configuration

Memory space

Memory space: 4GB addressable space apportioned into 16 slave slots, each of size 256MB

Address range seen by slave connected to huge (2GB) slot interface: 0x00000000 - 0x7FFFFFFF [✓ 0x80000000 - 0xFFFFFFFF]

Allocate memory space to combined region slave

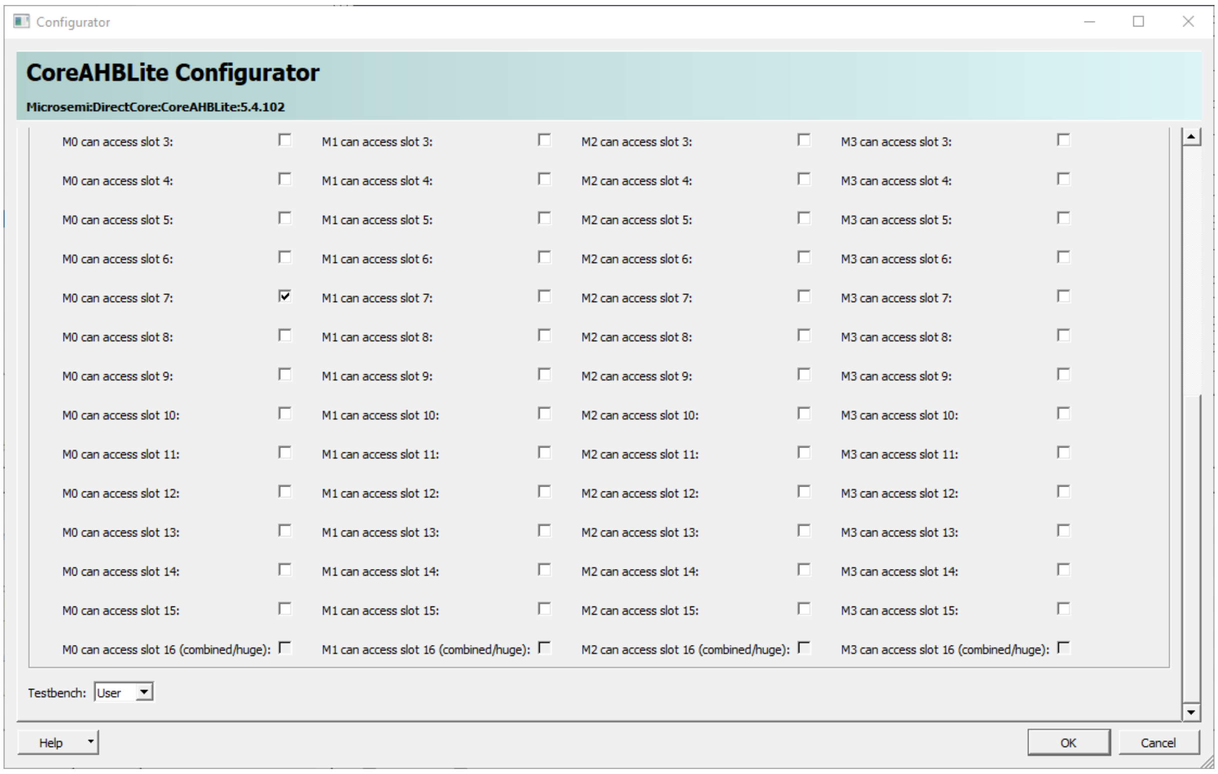
Slot 0: ☐	Slot 1: ☐	Slot 2: ☐	Slot 3: ☐
Slot 4: ☐	Slot 5: ☐	Slot 6: ☐	Slot 7: ☐
Slot 8: ☐	Slot 9: ☐	Slot 10: ☐	Slot 11: ☐
Slot 12: ☐	Slot 13: ☐	Slot 14: ☐	Slot 15: ☐

Enable Master access

M0 can access slot 0:	☐	M1 can access slot 0:	☐	M2 can access slot 0:	☐	M3 can access slot 0:	☐
M0 can access slot 1:	☐	M1 can access slot 1:	☐	M2 can access slot 1:	☐	M3 can access slot 1:	☐
M0 can access slot 2:	☐	M1 can access slot 2:	☐	M2 can access slot 2:	☐	M3 can access slot 2:	☐
M0 can access slot 3:	☐	M1 can access slot 3:	☐	M2 can access slot 3:	☐	M3 can access slot 3:	☐
M0 can access slot 4:	☐	M1 can access slot 4:	☐	M2 can access slot 4:	☐	M3 can access slot 4:	☐
M0 can access slot 5:	☐	M1 can access slot 5:	☐	M2 can access slot 5:	☐	M3 can access slot 5:	☐

Help | OK | Cancel

Figure 33: CoreAHBLite_0 Configuration



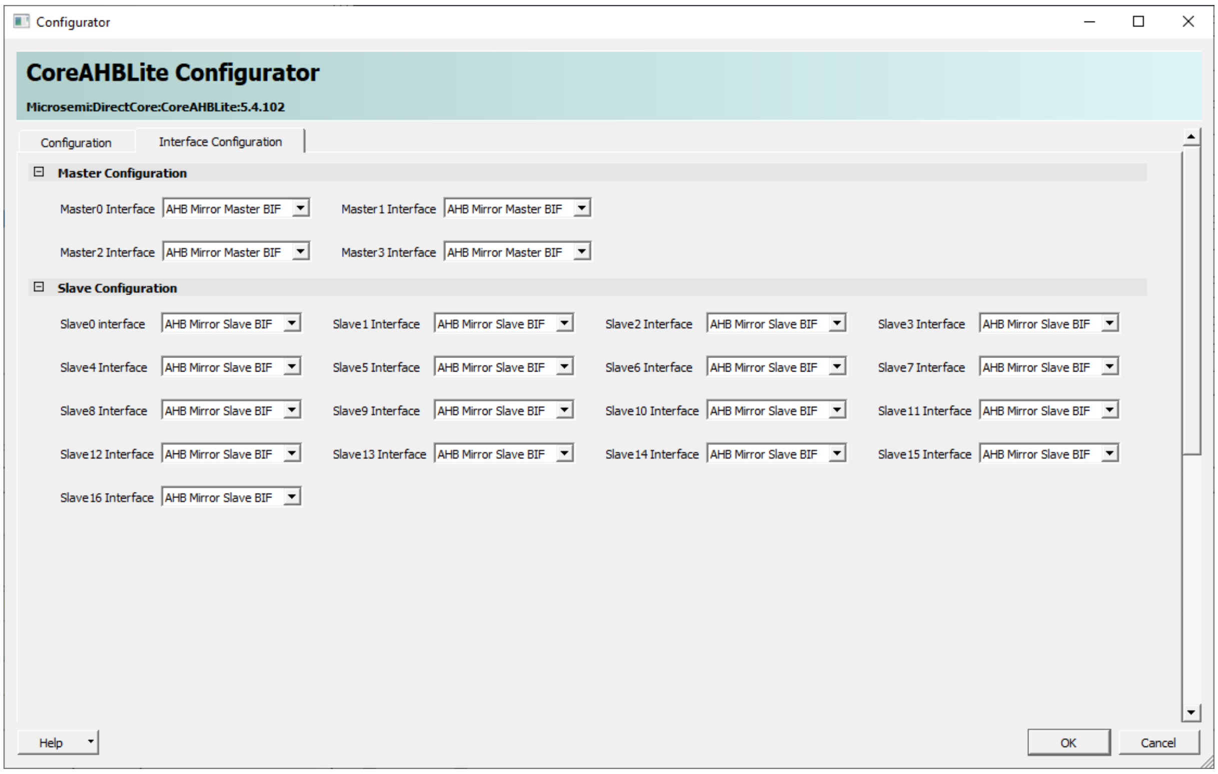
CoreAHBLite Configurator

Microsemi:DirectCore:CoreAHBLite:5.4.102

M0 can access slot 3:	☐	M1 can access slot 3:	☐	M2 can access slot 3:	☐	M3 can access slot 3:	☐
M0 can access slot 4:	☐	M1 can access slot 4:	☐	M2 can access slot 4:	☐	M3 can access slot 4:	☐
M0 can access slot 5:	☐	M1 can access slot 5:	☐	M2 can access slot 5:	☐	M3 can access slot 5:	☐
M0 can access slot 6:	☐	M1 can access slot 6:	☐	M2 can access slot 6:	☐	M3 can access slot 6:	☐
M0 can access slot 7:	☑	M1 can access slot 7:	☐	M2 can access slot 7:	☐	M3 can access slot 7:	☐
M0 can access slot 8:	☐	M1 can access slot 8:	☐	M2 can access slot 8:	☐	M3 can access slot 8:	☐
M0 can access slot 9:	☐	M1 can access slot 9:	☐	M2 can access slot 9:	☐	M3 can access slot 9:	☐
M0 can access slot 10:	☐	M1 can access slot 10:	☐	M2 can access slot 10:	☐	M3 can access slot 10:	☐
M0 can access slot 11:	☐	M1 can access slot 11:	☐	M2 can access slot 11:	☐	M3 can access slot 11:	☐
M0 can access slot 12:	☐	M1 can access slot 12:	☐	M2 can access slot 12:	☐	M3 can access slot 12:	☐
M0 can access slot 13:	☐	M1 can access slot 13:	☐	M2 can access slot 13:	☐	M3 can access slot 13:	☐
M0 can access slot 14:	☐	M1 can access slot 14:	☐	M2 can access slot 14:	☐	M3 can access slot 14:	☐
M0 can access slot 15:	☐	M1 can access slot 15:	☐	M2 can access slot 15:	☐	M3 can access slot 15:	☐
M0 can access slot 16 (combined/huge):	☐	M1 can access slot 16 (combined/huge):	☐	M2 can access slot 16 (combined/huge):	☐	M3 can access slot 16 (combined/huge):	☐

Testbench: User

Figure 34: CoreAHBLite_0 Configuration cont. ...



CoreAHBLite Configurator

Microsemi:DirectCore:CoreAHBLite:5.4.102

Master Configuration

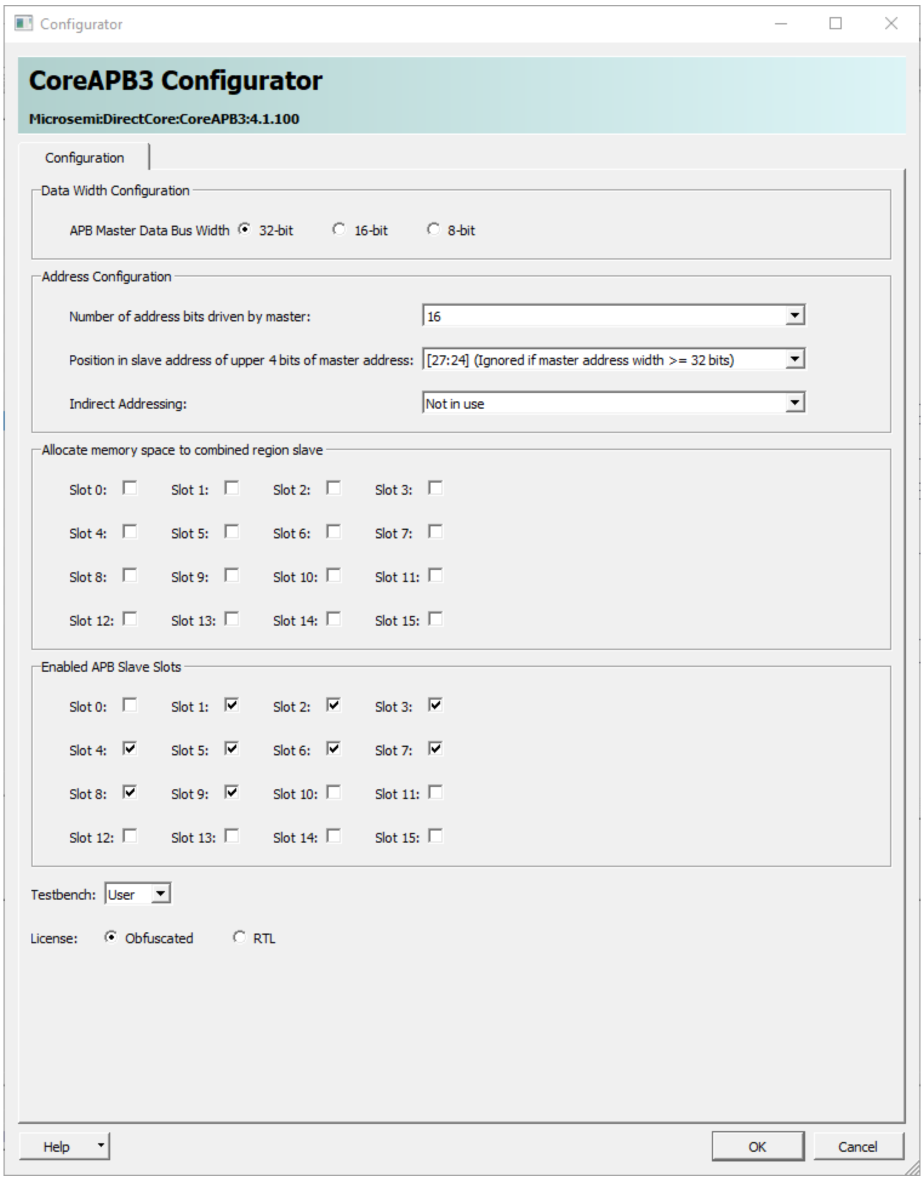
Master0 Interface	AHB Mirror Master BIF	Master1 Interface	AHB Mirror Master BIF
Master2 Interface	AHB Mirror Master BIF	Master3 Interface	AHB Mirror Master BIF

Slave Configuration

Slave0 interface	AHB Mirror Slave BIF	Slave1 Interface	AHB Mirror Slave BIF	Slave2 Interface	AHB Mirror Slave BIF	Slave3 Interface	AHB Mirror Slave BIF
Slave4 Interface	AHB Mirror Slave BIF	Slave5 Interface	AHB Mirror Slave BIF	Slave6 Interface	AHB Mirror Slave BIF	Slave7 Interface	AHB Mirror Slave BIF
Slave8 Interface	AHB Mirror Slave BIF	Slave9 Interface	AHB Mirror Slave BIF	Slave10 Interface	AHB Mirror Slave BIF	Slave11 Interface	AHB Mirror Slave BIF
Slave12 Interface	AHB Mirror Slave BIF	Slave13 Interface	AHB Mirror Slave BIF	Slave14 Interface	AHB Mirror Slave BIF	Slave15 Interface	AHB Mirror Slave BIF
Slave16 Interface	AHB Mirror Slave BIF						

Figure 35: CoreAHBLite_0 Interface Configuration

3.3.3.5 IP Core CoreAPB3_0


Configurator

CoreAPB3 Configurator

Microsemi:DirectCore:CoreAPB3:4.1.100

Configuration

Data Width Configuration

APB Master Data Bus Width [✓ 32-bit] 16-bit 8-bit

Address Configuration

Number of address bits driven by master:	16
Position in slave address of upper 4 bits of master address:	[27:24] (Ignored if master address width >= 32 bits)
Indirect Addressing:	Not in use

Allocate memory space to combined region slave

Slot 0: ☐	Slot 1: ☐	Slot 2: ☐	Slot 3: ☐
Slot 4: ☐	Slot 5: ☐	Slot 6: ☐	Slot 7: ☐
Slot 8: ☐	Slot 9: ☐	Slot 10: ☐	Slot 11: ☐
Slot 12: ☐	Slot 13: ☐	Slot 14: ☐	Slot 15: ☐

Enabled APB Slave Slots

Slot 0: ☐	Slot 1: ✓	Slot 2: ✓	Slot 3: ✓
Slot 4: ✓	Slot 5: ✓	Slot 6: ✓	Slot 7: ✓
Slot 8: ✓	Slot 9: ✓	Slot 10: ☐	Slot 11: ☐
Slot 12: ☐	Slot 13: ☐	Slot 14: ☐	Slot 15: ☐

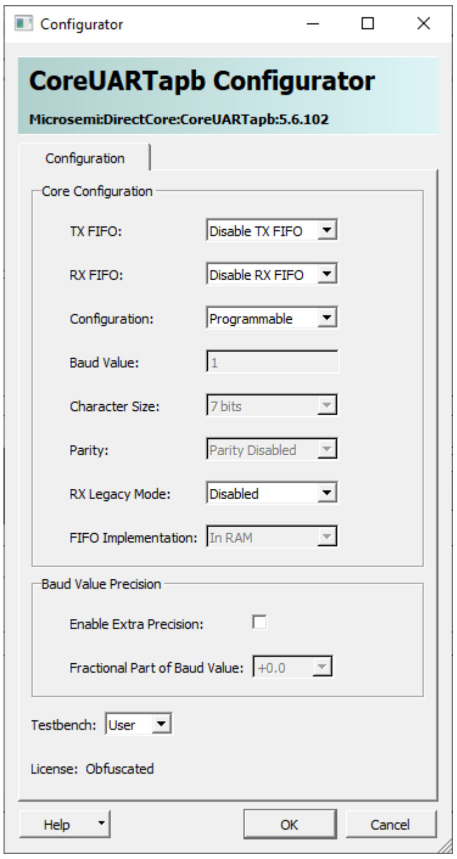
Testbench: User

License: [✓ Obfuscated] RTL

Help OK Cancel

Figure 36: CoreAPB3_0 Configuration

3.3.3.6 IP Core CoreUARTapb_0



CoreUARTapb Configurator

Microsemi:DirectCore:CoreUARTapb:5.6.102

Core Configuration

TX FIFO:	Disable TX FIFO
RX FIFO:	Disable RX FIFO
Configuration:	Programmable
Baud Value:	1
Character Size:	7 bits
Parity:	Parity Disabled
RX Legacy Mode:	Disabled
FIFO Implementation:	In RAM

Baud Value Precision

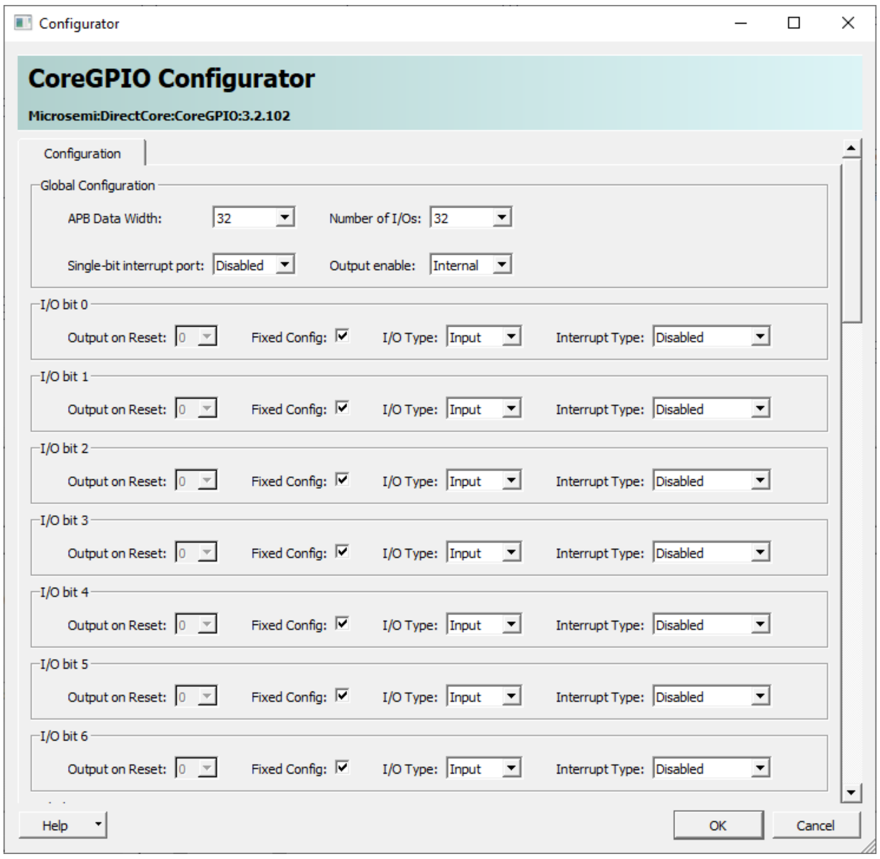
Enable Extra Precision:	☐
Fractional Part of Baud Value:	+0.0

Testbench: User

License: Obfuscated

Figure 37: CoreUARTapb_0 Configuration

3.3.3.7 IP Core CoreGPIO_IN


Configurator

CoreGPIO Configurator

Microsemi:DirectCore:CoreGPIO:3.2.102

Configuration

Global Configuration

APB Data Width: 32 Number of I/Os: 32

Single-bit interrupt port: Disabled Output enable: Internal

I/O bit 0
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

I/O bit 1
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

I/O bit 2
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

I/O bit 3
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

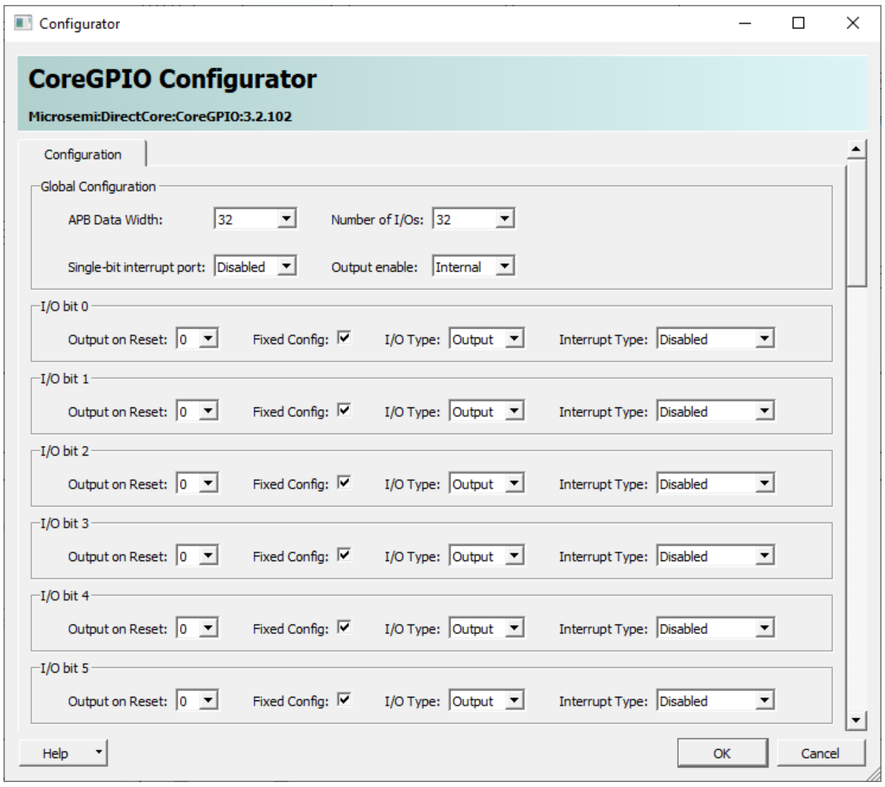
I/O bit 4
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

I/O bit 5
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

I/O bit 6
Output on Reset: 0 Fixed Config: ✓ I/O Type: Input Interrupt Type: Disabled

Figure 38: CoreGPIO_IN Configuration (all IOs have the same configuration)

3.3.3.8 IP Core CoreGPIO_OUT



CoreGPIO Configurator

Microsemi:DirectCore:CoreGPIO:3.2.102

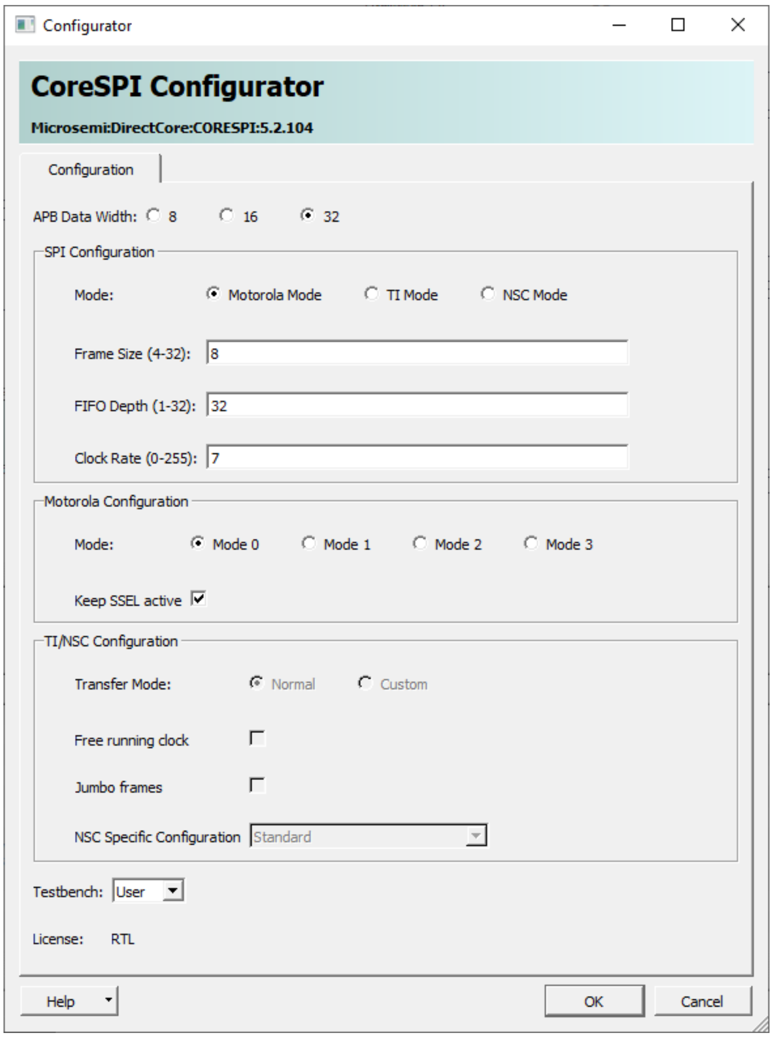
Global Configuration

APB Data Width: 32
Number of I/Os: 32
Single-bit interrupt port: Disabled
Output enable: Internal

I/O bit	Output on Reset	Fixed Config	I/O Type	Interrupt Type
I/O bit 0	0	✓	Output	Disabled
I/O bit 1	0	✓	Output	Disabled
I/O bit 2	0	✓	Output	Disabled
I/O bit 3	0	✓	Output	Disabled
I/O bit 4	0	✓	Output	Disabled
I/O bit 5	0	✓	Output	Disabled

Figure 39: CoreGPIO_OUT Configuration (all IOs have the same configuration)

3.3.3.9 IP Core CORESPI_0


Configurator

CoreSPI Configurator

Microsemi:DirectCore:CORESPI:5.2.104

Configuration

APB Data Width: 8 16 [✓ 32]

SPI Configuration

Mode: [✓ Motorola Mode] TI Mode NSC Mode

Frame Size (4-32): 8

FIFO Depth (1-32): 32

Clock Rate (0-255): 7

Motorola Configuration

Mode: [✓ Mode 0] Mode 1 Mode 2 Mode 3

Keep SSEL active ✓

TI/NSC Configuration

Transfer Mode: [✓ Normal] Custom

Free running clock ☐

Jumbo frames ☐

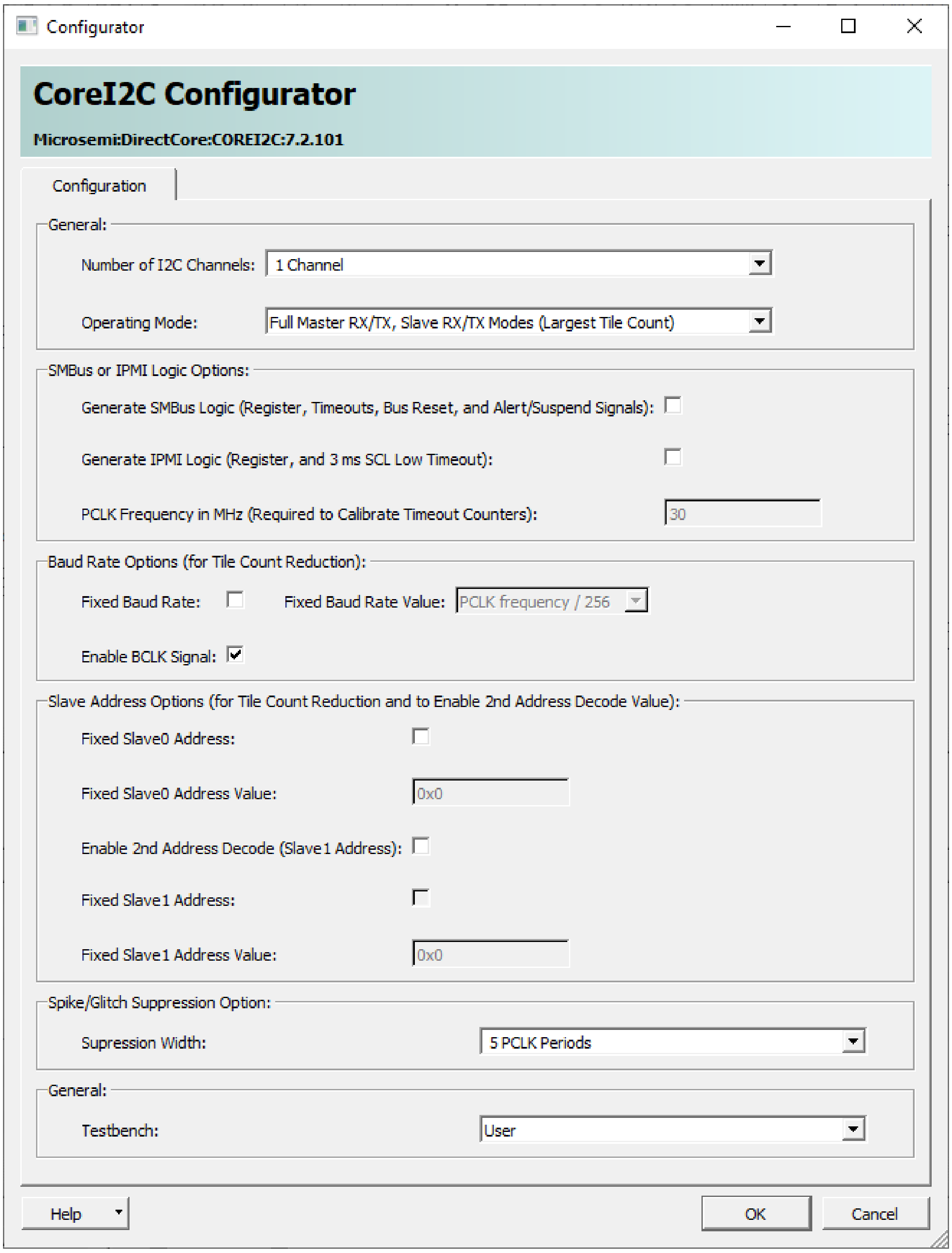
NSC Specific Configuration: Standard

Testbench: User

License: RTL

Figure 40: CORESPI_0 Configuration

3.3.3.10 IP Core COREI2C_0


Configurator

CoreI2C Configurator

Microsemi:DirectCore:COREI2C:7.2.101

Configuration

General:

Number of I2C Channels: 1 Channel

Operating Mode: Full Master RX/TX, Slave RX/TX Modes (Largest Tile Count)

SMBus or IPMI Logic Options:

Generate SMBus Logic (Register, Timeouts, Bus Reset, and Alert/Suspend Signals): ☐

Generate IPMI Logic (Register, and 3 ms SCL Low Timeout): ☐

PCLK Frequency in MHz (Required to Calibrate Timeout Counters): 30

Baud Rate Options (for Tile Count Reduction):

Fixed Baud Rate: ☐ Fixed Baud Rate Value: PCLK frequency / 256

Enable BCLK Signal: ☑

Slave Address Options (for Tile Count Reduction and to Enable 2nd Address Decode Value):

Fixed Slave0 Address: ☐

Fixed Slave0 Address Value: 0x0

Enable 2nd Address Decode (Slave1 Address): ☐

Fixed Slave1 Address: ☐

Fixed Slave1 Address Value: 0x0

Spike/Glitch Suppression Option:

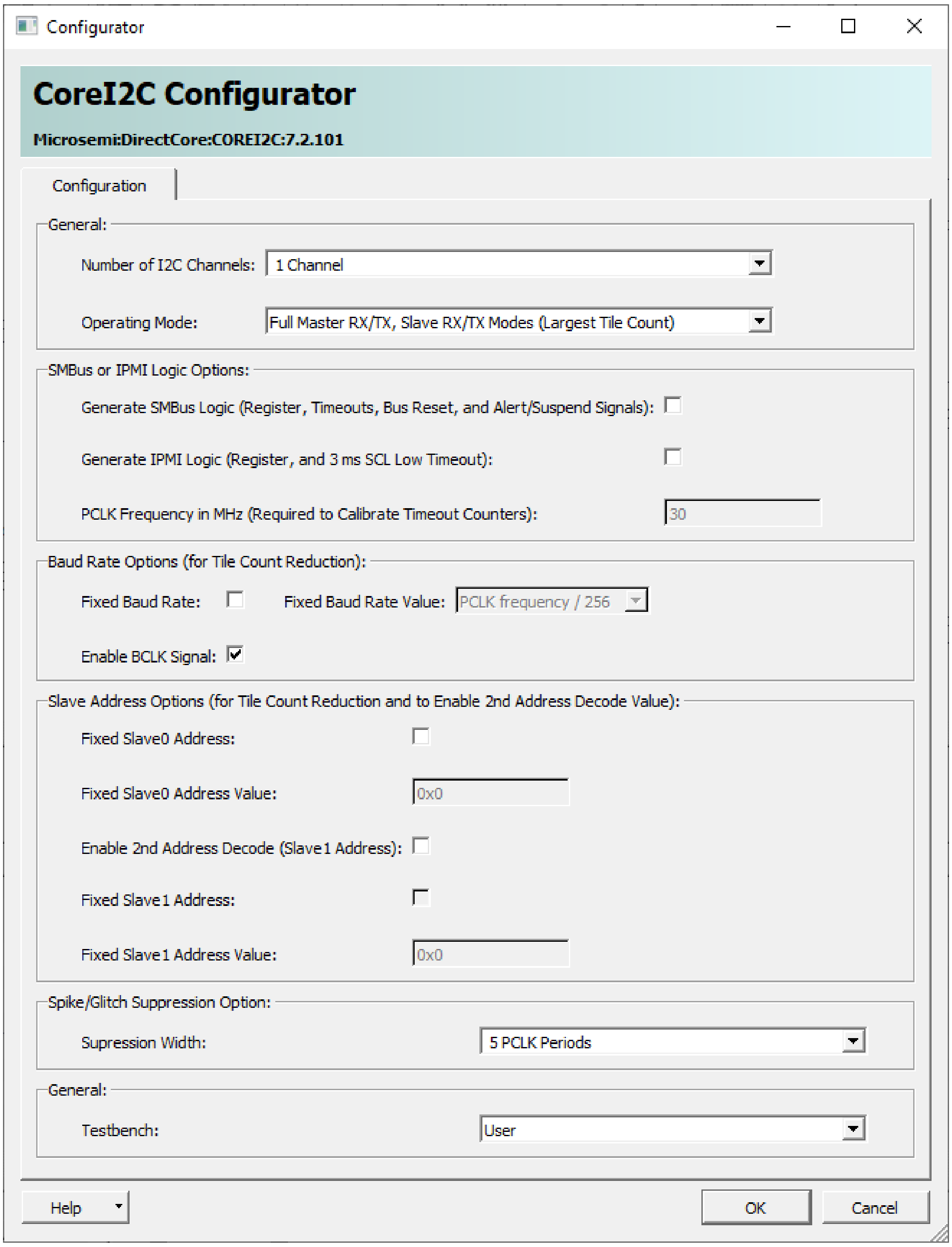
Supression Width: 5 PCLK Periods

General:

Testbench: User

Figure 41: COREI2C_0 Configuration

3.3.3.11 IP Core COREI2C_1


Configurator

CoreI2C Configurator

Microsemi:DirectCore:COREI2C:7.2.101

Configuration

General:

Number of I2C Channels: 1 Channel

Operating Mode: Full Master RX/TX, Slave RX/TX Modes (Largest Tile Count)

SMBus or IPMI Logic Options:

Generate SMBus Logic (Register, Timeouts, Bus Reset, and Alert/Suspend Signals): ☐

Generate IPMI Logic (Register, and 3 ms SCL Low Timeout): ☐

PCLK Frequency in MHz (Required to Calibrate Timeout Counters): 30

Baud Rate Options (for Tile Count Reduction):

Fixed Baud Rate: ☐ Fixed Baud Rate Value: PCLK frequency / 256

Enable BCLK Signal: ☑

Slave Address Options (for Tile Count Reduction and to Enable 2nd Address Decode Value):

Fixed Slave0 Address: ☐

Fixed Slave0 Address Value: 0x0

Enable 2nd Address Decode (Slave1 Address): ☐

Fixed Slave1 Address: ☐

Fixed Slave1 Address Value: 0x0

Spike/Glitch Suppression Option:

Supression Width: 5 PCLK Periods

General:

Testbench: User

Help OK Cancel

Figure 42: COREI2C_1 Configuration

3.3.4 Smart Design video_isp_pipe

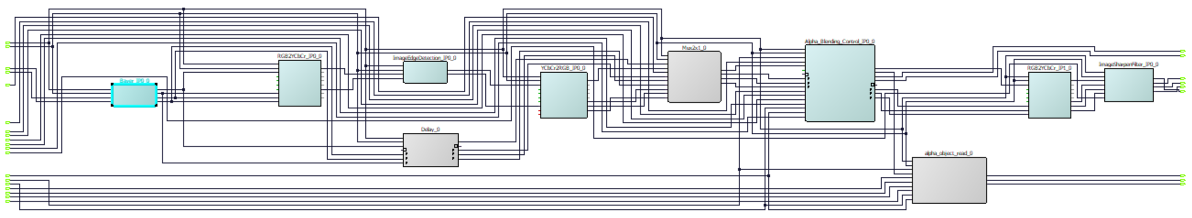
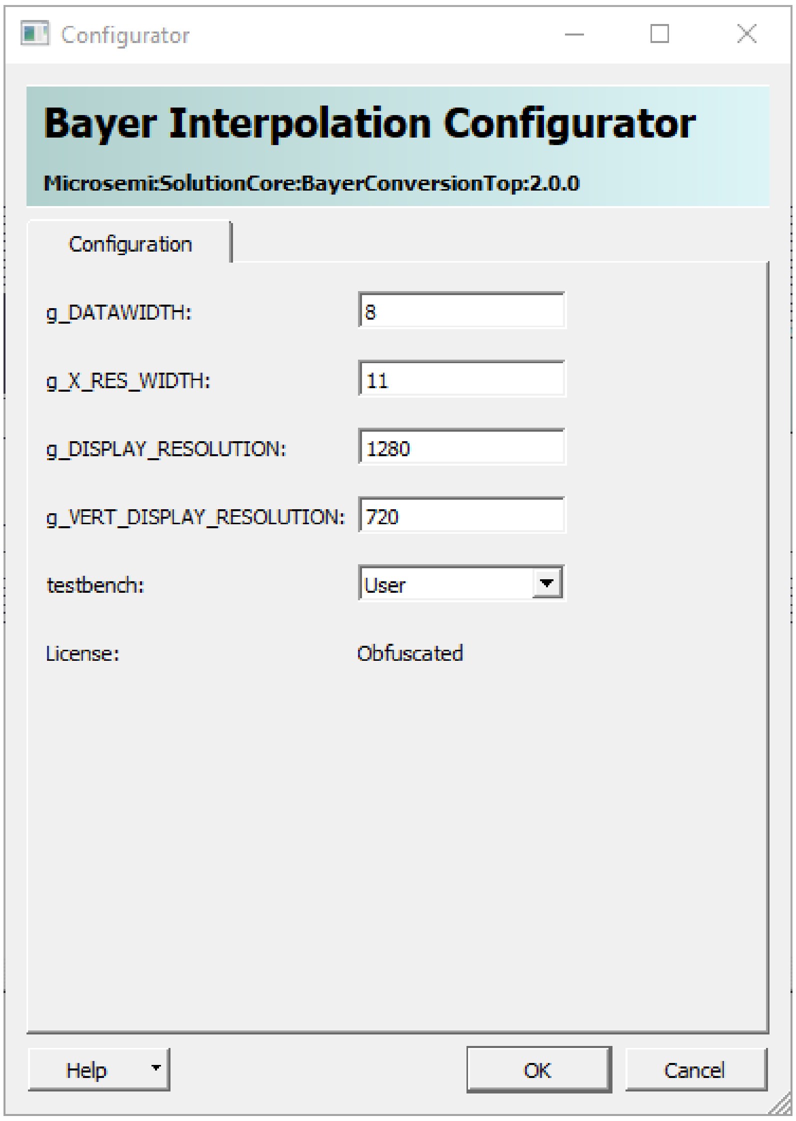


Figure 43: SmartDesign video_isp_pipe

3.3.4.1 IP Core Bayer_IP0_0



Configurator

Bayer Interpolation Configurator

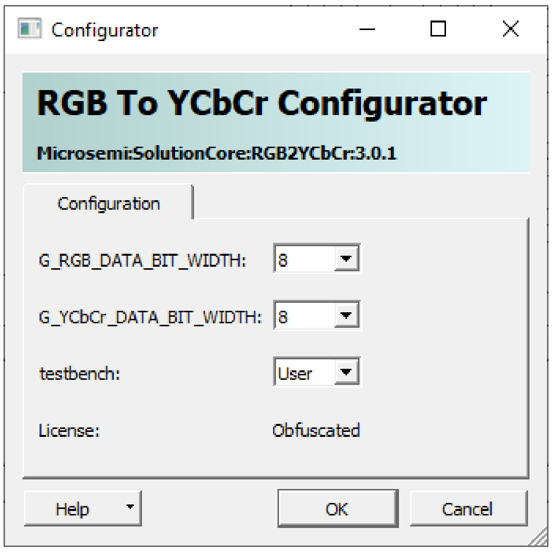
Microsemi:SolutionCore:BayerConversionTop:2.0.0

Configuration

g_DATAWIDTH:	8
g_X_RES_WIDTH:	11
g_DISPLAY_RESOLUTION:	1280
g_VERT_DISPLAY_RESOLUTION:	720
testbench:	User
License:	Obfuscated

Figure 44: Bayer_IP0_0 Configuration

3.3.4.2 IP Core RGB2YCbCr_IP0_0



RGB To YCbCr Configurator

Microsemi:SolutionCore:RGB2YCbCr:3.0.1

Configuration

G_RGB_DATA_BIT_WIDTH: 8

G_YCbCr_DATA_BIT_WIDTH: 8

testbench: User

License: Obfuscated

Figure 45: RGB2YCbCr_IP0_0 Configuration

3.3.4.3 IP Core ImageEdgeDetection_IP0_0

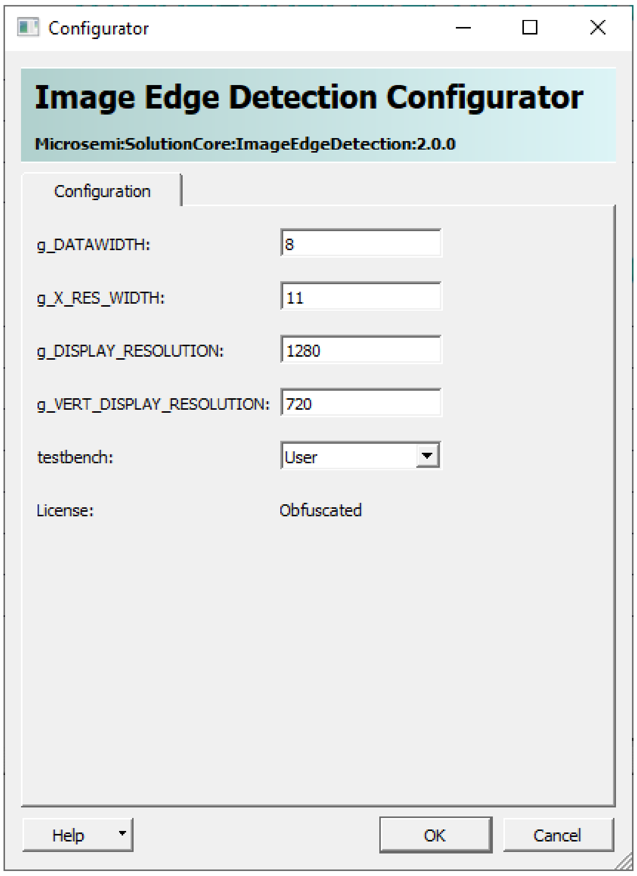


Image Edge Detection Configurator

Microsemi:SolutionCore:ImageEdgeDetection:2.0.0

Configuration

g_DATAWIDTH: 8

g_X_RES_WIDTH: 11

g_DISPLAY_RESOLUTION: 1280

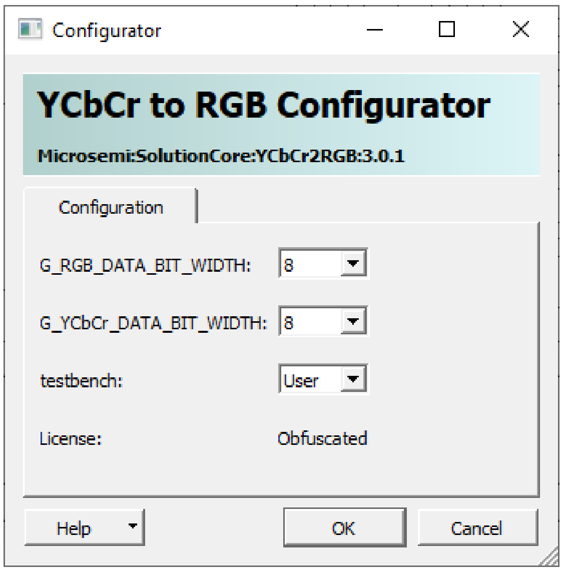
g_VERT_DISPLAY_RESOLUTION: 720

testbench: User

License: Obfuscated

Figure 46: ImageEdgeDetection_IP0_0 Configuration

3.3.4.4 IP Core YCbCr2RGB_IP0_0


Configurator

YCbCr to RGB Configurator

Microsemi:SolutionCore:YCbCr2RGB:3.0.1

Configuration

G_RGB_DATA_BIT_WIDTH: 8

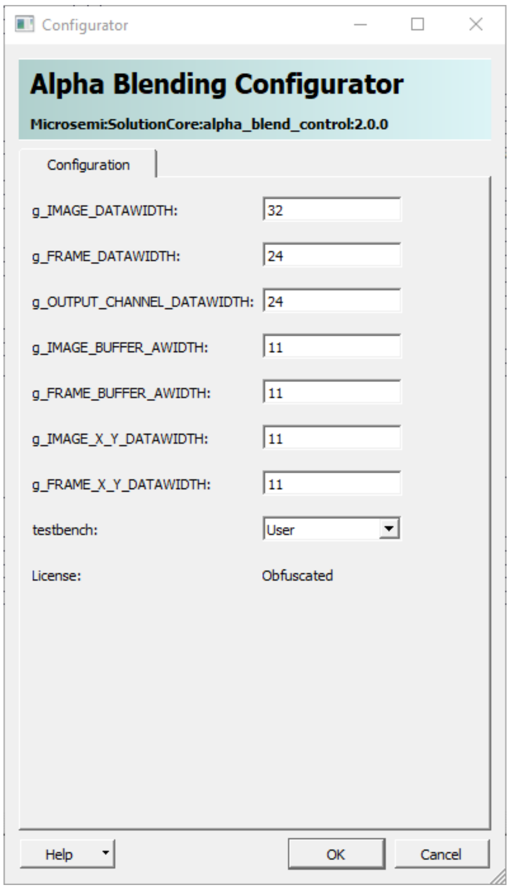
G_YCbCr_DATA_BIT_WIDTH: 8

testbench: User

License: Obfuscated

Figure 47: YCbCr2RGB_IP0_0 Configuration

3.3.4.5 IP Core Alpha_Blending_Control_IP0_0


Configurator

Alpha Blending Configurator

Microsemi:SolutionCore:alpha_blend_control:2.0.0

Configuration

g_IMAGE_DATAWIDTH: 32

g_FRAME_DATAWIDTH: 24

g_OUTPUT_CHANNEL_DATAWIDTH: 24

g_IMAGE_BUFFER_AWIDTH: 11

g_FRAME_BUFFER_AWIDTH: 11

g_IMAGE_X_Y_DATAWIDTH: 11

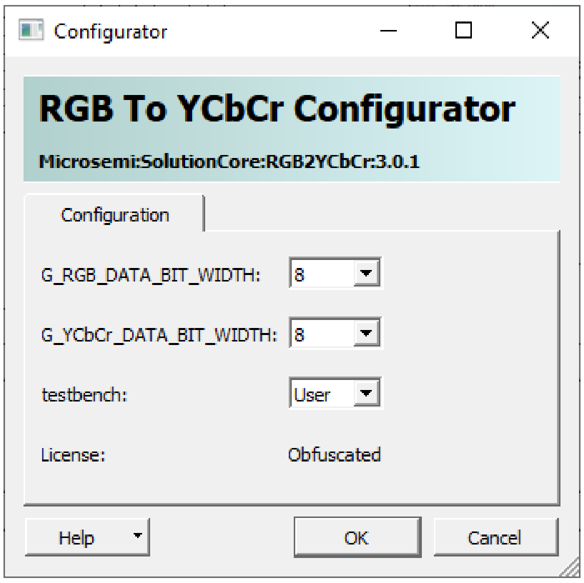
g_FRAME_X_Y_DATAWIDTH: 11

testbench: User

License: Obfuscated

Figure 48: Alpha_Blending_Control_IP0_0 Configuration

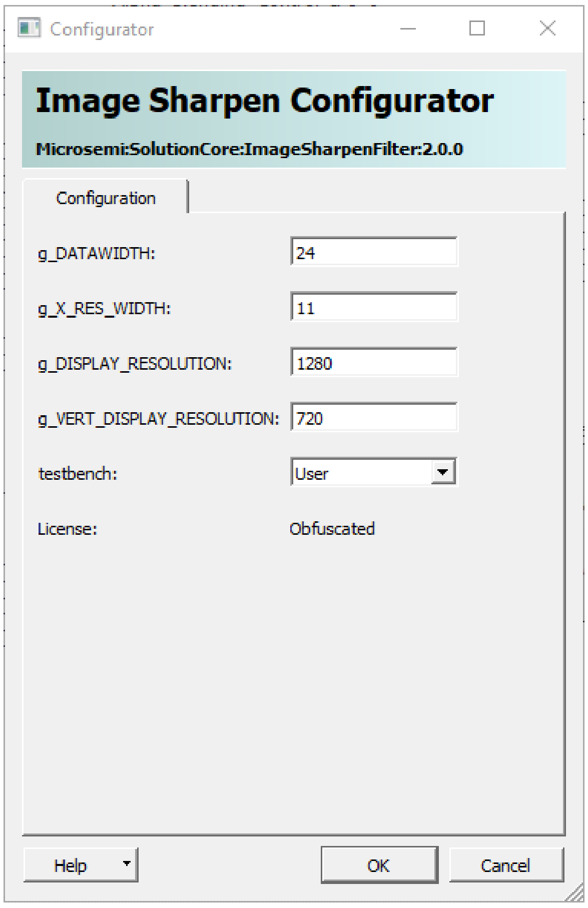
3.3.4.6 IP Core RGB2YCbCr_IP1_0


Configurator
RGB To YCbCr Configurator
Microsemi:SolutionCore:RGB2YCbCr:3.0.1
Configuration
Help
OK
Cancel

G_RGB_DATA_BIT_WIDTH: 8
G_YCbCr_DATA_BIT_WIDTH: 8
testbench: User
License: Obfuscated

Figure 49: RGB2YCbCr_IP1_0 Configuration

3.3.4.7 IP Core ImageSharpenFilter_IP0_0


Configurator
Image Sharpen Configurator
Microsemi:SolutionCore:ImageSharpenFilter:2.0.0
Configuration
Help
OK
Cancel

g_DATAWIDTH: 24
g_X_RES_WIDTH: 11
g_DISPLAY_RESOLUTION: 1280
g_VERT_DISPLAY_RESOLUTION: 720
testbench: User
License: Obfuscated

Figure 50: ImageSharpenFilter_IP0_0 Configuration

3.4 Running the Design

The design uses a MIV processor. The release is programmed in NVM.

The software project can be found in the MiV_Workspace

If programmed correctly, the camera image appears on the monitor after powering the board.

Use the GUI to adjust the image enhancements or run the edge Detection.

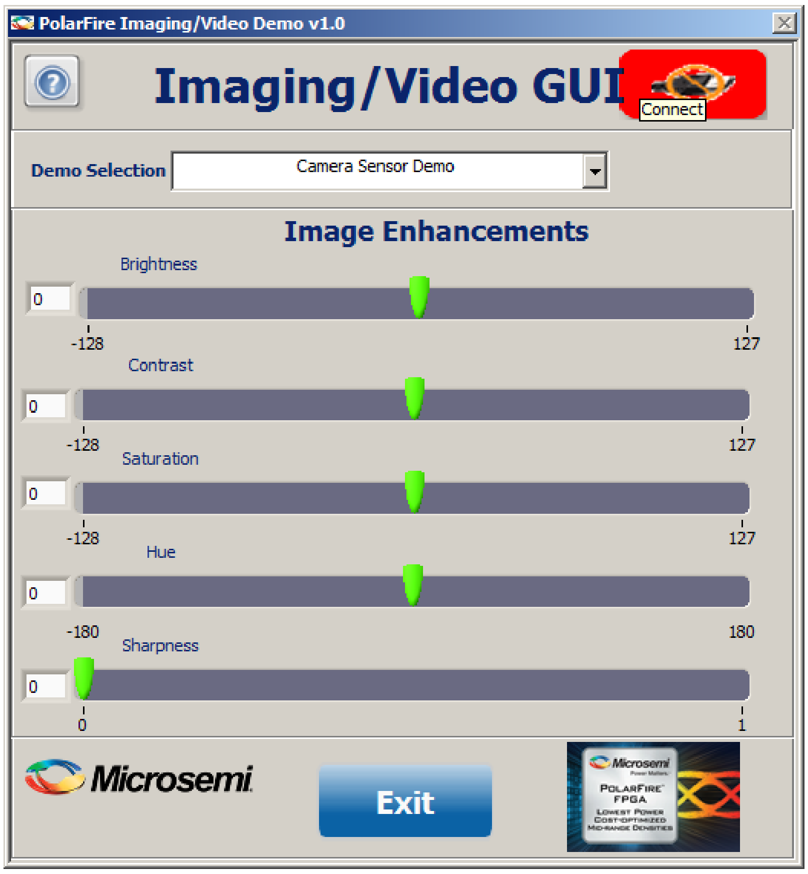


Figure 51: Imaging/Video GUI