

Everest-10G-Webserver-Demo

Getting Started

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	edited:	S. Rieche	Date:	2019-03-19
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Contents

1. Revision History	5
1.1 Revision 1.2.....	5
1.2 Revision 1.1.....	5
1.3 Revision 1.0.....	5
2. Getting Started	6
2.1 Prerequisites.....	6
2.2 Handling the Board.....	7
2.3 Board-Setup Revision PROTO.....	7
2.3.1 Toggle-Switch S1 – PCIe	7
2.3.2 Toggle -Switch S5 – SC SPI-Flash enable	7
2.3.3 DIP-Switch S8 – FMC Voltage Selector.....	7
2.3.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage.....	7
2.4 Board-Setup Revision A and B	8
2.4.1 Toggle-Switch S1 – PCIe	8
2.4.2 Toggle -Switch S5 – SC SPI-Flash enable	8
2.4.3 DIP-Switch S8 – FMC Voltage Selector.....	8
2.4.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage.....	8
2.5 Powering up the Board.....	9
3. Demo Design	10
3.1 SFP+ related differences between Everest DEV Board PROTO and Revision A and B	10
3.2 Prerequisites.....	12
3.3 Design Implementation	12
3.4 Running the Design.....	15

Figures

Figure 1: Everest Board.....	9
Figure 2: SFP+ hardware Everest DEV Board PROTO	10
Figure 3: SFP+ hardware Everest DEV Board Rev. A and B.....	11
Figure 4: Design Implementation	13
Figure 5: Webserver Main Page.....	16
Figure 6: Text Terminal Mode Input	17
Figure 7: Text Terminal Output.....	17
Figure 8: LED Mode	18
Figure 9: Google Search Bar	18

Tables

Table 1: Software / IP Requirements 12

Table 2: Hardware Design Clock Frequencies 13

1. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.2

The document was updated for Libero SoC v12.0.

1.2 Revision 1.1

The document was updated for the use of Everest DEV Board Rev. A and B.

The document was updated for Libero SoC PolarFire v2.2.

1.3 Revision 1.0

Revision 1.0 is the first publication of this document.

2. Getting Started

The PolarFire® FPGA 10G Ethernet feature is compliant with the IEEE 802.3ae standard, which supports data transfer rates of up to 10.3125 Gbps. Advantages offered by PolarFire FPGAs for building 10G Ethernet solutions include the use of low-power transceivers, low-power FPGA fabric, and SyncE-compliant jitter attenuation.

In PolarFire devices, the 10G Ethernet feature is implemented using the CORE10GMAC soft IP media access control (MAC) core, which can be configured either in 10GBASE-KR mode or 10GBASE-R mode.

2.1 Prerequisites

For the Everest 10G Webserver Demo the following is needed:

Item	Quantity
Everest DEV Board	1
12 V / 5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for UART / Programming interface to PC	1
Intel X520-DA2 10GbE Adapter PCIE	1
Finisar FTLX8574D3BCV 10G Optical Transceiver	2
Tripp Lite N820-03M Optical Duplex LC Cable	1
Free one-year Libero Silver software license	1

Note 1: The Everest DEV Board offers an on-board FlashPro5 programmer, which can be used to program and debug with Identify, SmartDebug and embedded application software using SoftConsole.

Note 2: There are differences between Everest Dev Board PROTO and Rev. A and B concerning the configuration of the SFP+ interface that are described in chapter 3.1.

2.2 Handling the Board

Pay attention to the following points while handling or operating the board:

Handle the board with electrostatic discharge (ESD) precautions to avoid damage.

For information about ESD precautions see

https://www.microsemi.com/documentportal/doc_view/126483-esd-appnote.

2.3 Board-Setup Revision PROTO

2.3.1 Toggle-Switch S1 – PCIe

Warning: S1-1 and S1-2 must not be at position on at the same time!

SWITCH ON	PCIe LANES
S1-1	x1
S1-2	x4

2.3.2 Toggle -Switch S5 – SC SPI-Flash enable

Warning: S5-1 and S5-2 must not be at position on at the same time!

SWITCH ON	SC SPI-FLASH
S5-1	ENABLE
S5-2	DISABLE

2.3.3 DIP-Switch S8 – FMC Voltage Selector

Warning: S8-1 to S8-4 must not be at position on at the same time!

SWITCH ON	FMC VOLTAGE
S8-1	3.3 V
S8-2	2.5 V
S8-3	1.8 V
S8-4	undefined (not connected)

2.3.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

Warning: S9-1 and S9-2 must not be at position on at the same time!

SWITCH ON	VDDAUX2 & VDDAUX5
S9-1	2.5 V
S9-2	FMC voltage

2.4 Board-Setup Revision A and B

2.4.1 Toggle-Switch S1 – PCIe

SWITCH	PCIe LANES
S1-1 (marking)	x4
S1-2	x1

2.4.2 Toggle -Switch S5 – SC SPI-Flash enable

SWITCH	SC SPI-FLASH
S5-1 (marking)	DISABLE
S5-2	ENABLE

2.4.3 DIP-Switch S8 – FMC Voltage Selector

SWITCH	FMC VOLTAGE
S8-1 off, S8-2 off	1.8 V
S8-1 on, S8-2 off	2.5 V
S8-1 off, S8-2 on	undefined (not recommended)
S8-1 on, S8-2 on	3.3 V

2.4.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

SWITCH	VDDAUX2 & VDDAUX5
S9-1 (marking)	2.5 V
S9-2	FMC voltage

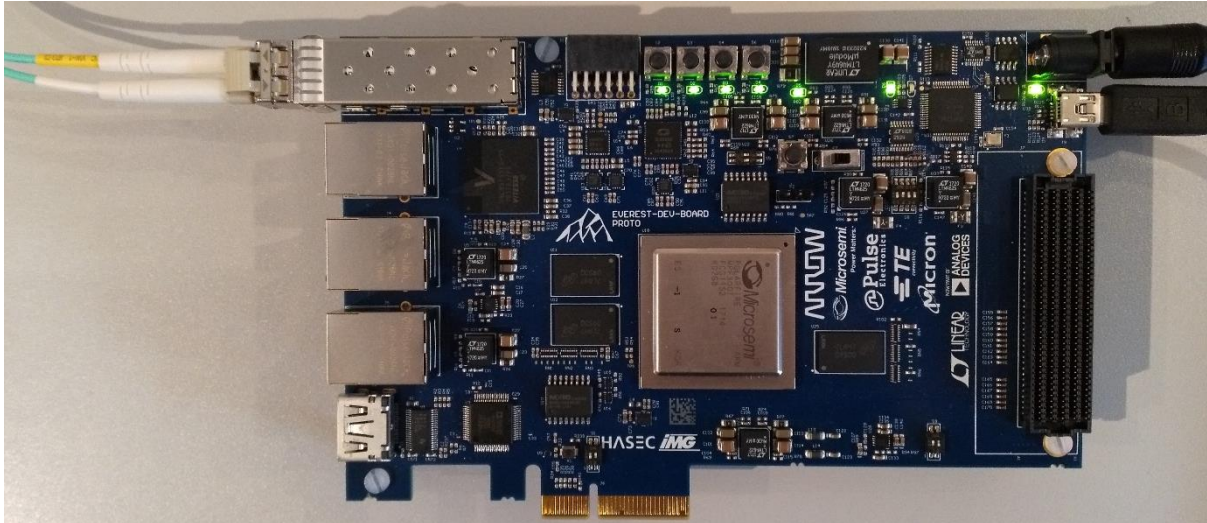


Figure 1: Everest Board

2.5 Powering up the Board

Insert the Finisar Optical Transceiver into the J1 connector (SFP+ module cage).

Connect the J1 connector to the Intel X520-DA2 10GbE Adapter using an optical fiber cable.

The Everest DEV Board is powered up using either the 12 V DC jack or the PCIe connector.

For programming connect it although with your computer using USB mini B connector J9.

3. Demo Design

3.1 SFP+ related differences between Everest DEV Board PROTO and Revision A and B

On Everest DEV Board PROTO the SFP+ signals *RX_LOS*, *RS0*, *RS1*, *TX_DIS* and *TX_FAULT* could only be accessed via the I2C I/O expander PCA9538 that is connected to the same I2C bus as the SFP+ interface itself.

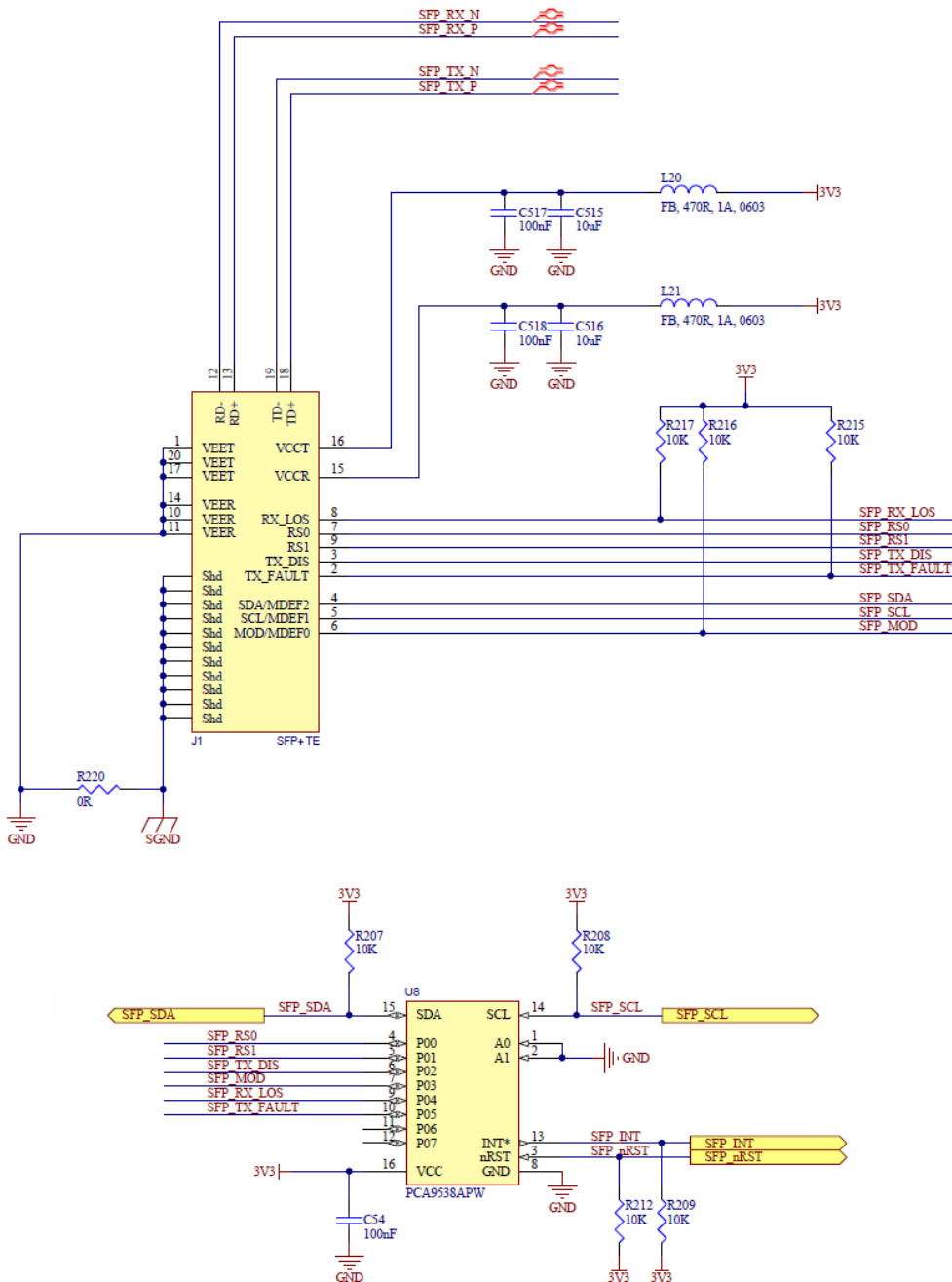


Figure 2: SFP+ hardware Everest DEV Board PROTO

3.2 Prerequisites

Software and IP core requirements are the same for Everest DEV Board PROTO and Rev. A and B.

Table 1: Software / IP Requirements

Software	Version
Libero SoC PolarFire	V12.0
Synplify Pro	N-2018.03M-SP1-1
FlashPro PolarFire	V2.0
IP	
CORE10GMAC	2.1.124 (BETA Version, comes with Project Files)
Transceiver Interface	1.0.231
CortexM1	3.0.100
PF_SRAM_ABHL_AXI	1.1.127
PF_XCVR_REF_CLK	1.0.103
PF_TX_PLL	2.0.002
PF_INIT_MONITOR	2.0.103
CoreAHBLite	5.3.101
CoreAHBTOAPB3	3.1.100
CoreAPB3	4.1.100
PF_CCC	1.0.115
CoreTimer	2.0.103
CoreUARTapb	5.6.102
CoreI2C	7.2.101
CoreGPIO	3.2.102

Before you start you have to make sure, that all cores are downloaded to your local vault.

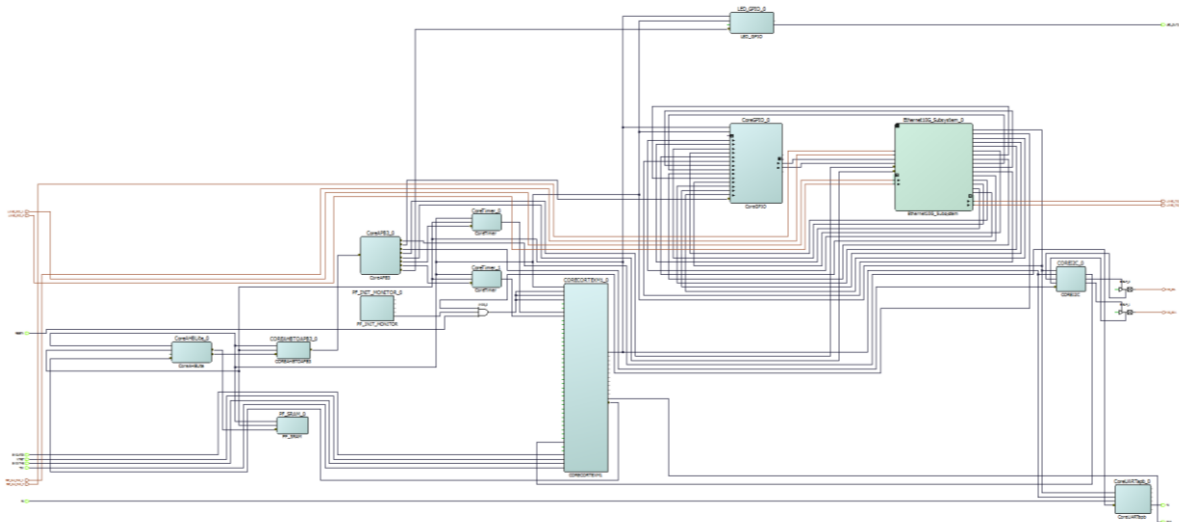
The CORE10GMAC-Core is provided in the Project File Archive (File "Actel_DirectCore_CORE10GMAC_2.1.124.cpz"). This Core should be imported from this local file.

3.3 Design Implementation

The following table lists the clock frequencies used in the design.

Table 2: Hardware Design Clock Frequencies

Clock	Frequency (MHz)
CDR reference clock	156.25
Transceiver bit clock	5156.25
I_SYS_CLOCK	156.25
I_CORE_TX_CLK	322.26
I_CORE_RX_CLK	322.26
HCLK / PCLK	100

**Figure 4: Design Implementation**

The top-level design implementation for Everest DEV Board Rev. A and B has an extra CoreGPIO called *SFP_CTRL* that receives the signal *SFP_MOD*, *SFP_TX_FAULT* and *SFP_RX_LOS*, including interrupt generation for those signals, and drives the signals *SFP_TX_DIS*, *SFP_RS0* and *SFP_RS1*.

The design is already fully implemented and ready to be programmed on the Everest Board. The board has to be connected with the power supply and to the PC with the USB cable. All drivers have to be installed (which should happen automatically when plugged in the first time) To program the design, there are two possibilities:

- Programming via Libero SoC: Programming is started with the “Run PROGRAM Action” Button in the Design Flow Pane
- Programming via FlashPro Software: For preproduction and production devices use the STAPL-file in the “Bitstream” folder. The STAPL-file for engineering samples is

located in the folder "Bitstream_ES". A new FlashPro project has to be generated and the programming file loaded into.

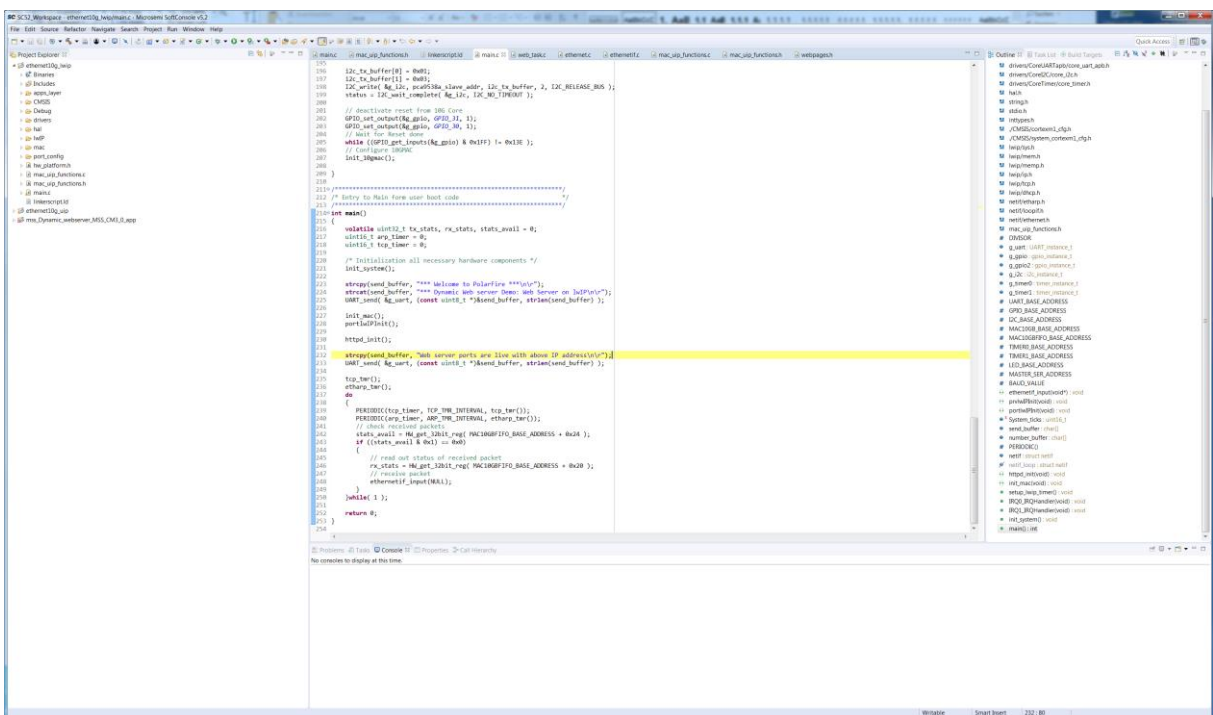
3.4 Running the Design

In Order to run the design, the CortexM1-Processor has to be loaded with the firmware. To do so, load the provided SoftConsole Workspace.

To choose between the two different configurations needed for Everest DEV Board PROTO or revision A and B, use the following software switch:

```
28
29 #define EVEREST_DEV_BOARD_REV_A_OR_B      1
30 ...
```

If you use either board revision A or B, set it to '1'. Otherwise set it to '0' and revision PROTO will be assumed.



The project “ethernet10g_lwip” provides a webserver application which is based on the lwip ip stack. The stack was modified to work with the proprietary FIFO, the CortexM1 processor uses to communicate with the 10GB Ethernet MAC Core.

The project is working with some hard-coded IP-Addresses:

- Board Address: 192.168.100.2
- Gateway Address: 192.168.100.1

These addresses can be modified in file “port_config/conf_eth.h” in lines 76 through 79 (board address) and lines 83 through 86 (gateway address). If the addresses are modified, a recompilation of the project is necessary.

A debug configuration is provided to download the firmware to the CortexM1 processor and start the webserver application.

After starting the application in debug mode, the webserver is reachable with a standard browser on the configured IP-Address:



For More Information about PolarFire products, refer to the Microsemi FPGA Products website:
<https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga>

Figure 5: Webserver Main Page

The application contains a text terminal mode, where a string can be sent to a Hyperterminal console. The Hyperterminal should be configured to the following parameters:

- Baud Rate 115200, 8 Databits, 1 Stopbit, no parity (8N1)
- COM-Port is visible in Device Manager (Windows)



Text Terminal Mode

String to display in Hyperterminal:

[Home](#)

Figure 6: Text Terminal Mode Input

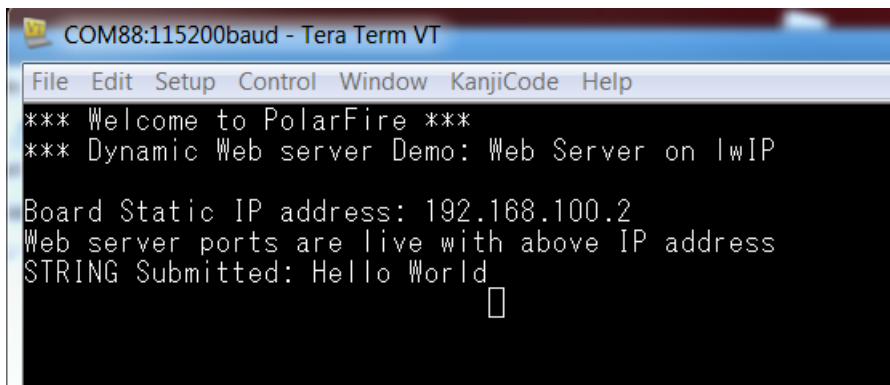


Figure 7: Text Terminal Output

The application contains a mode, where an inputted string controls the board LEDs. The number is interpreted as binary value and the LEDs are switched accordingly (e.g. 6d = 0110b => LED0 and LED3 are off, LED1 and LED2 are on)

Blinking LED's

LEDs on the board should blink once from 1 to 15

To blink LEDs manually enter any value between 1 to 15 :

Figure 8: LED Mode

The application contains one additional mode. It's a google search bar. Type in some text and hit the "Google Search" Button. A new window will appear with the search results.

Note: This mode will only work if the Everest Board is in a network with access to the internet! It's not sufficient to have a connection to a PC; A 10Gb router will be needed!

Loading

The Web

Figure 9: Google Search Bar