

ARROW Polarfire Everest Development Board

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M1
Rubber Feet
Rubber Feet

M2
Rubber Feet
Rubber Feet

M3
Rubber Feet
Rubber Feet

M4
Rubber Feet
Rubber Feet

M5
USB Cable
USB Cable

M6
Power Supply
AC/DC DESKTOP ADAPTER 12V 60W

M7
Supply Cable
AC CORD EUROPE C7 18AWG 6' BLACK


M8
Power Adapter
Adapter, EU-Stecker mit 2 Pins zu UK-Stecker, schneller Anschluss

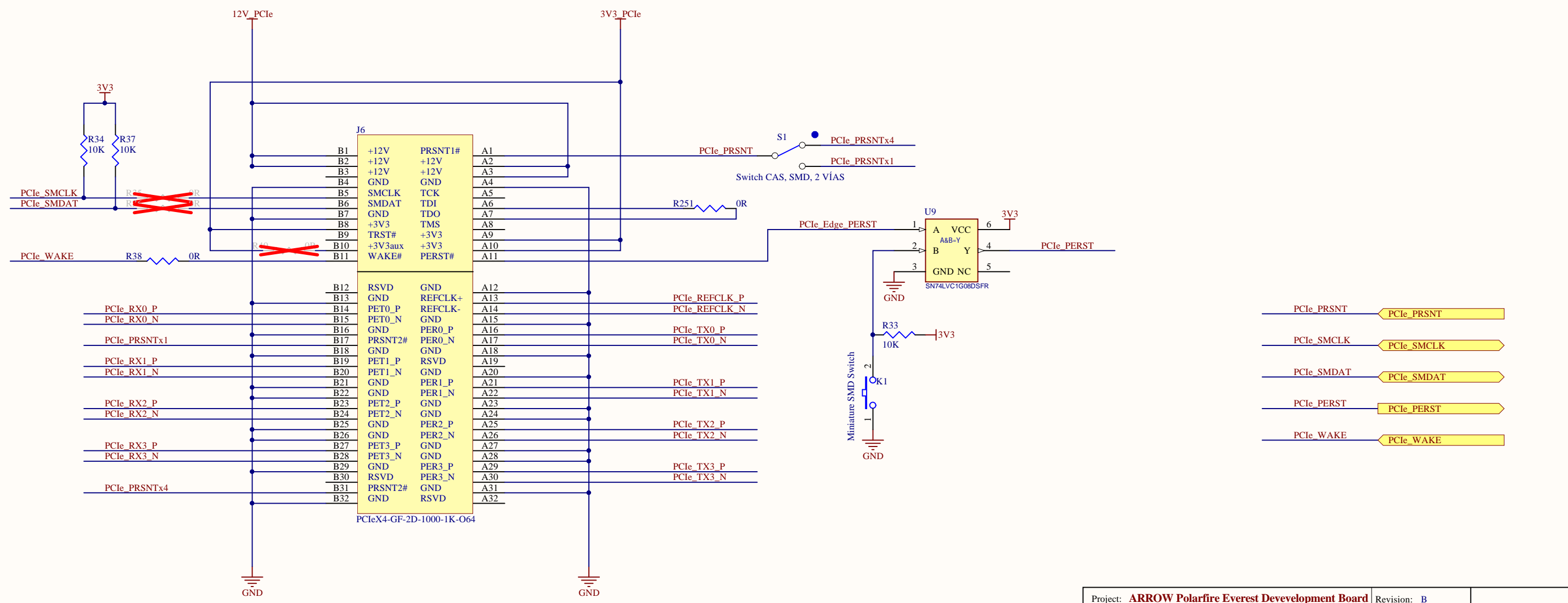
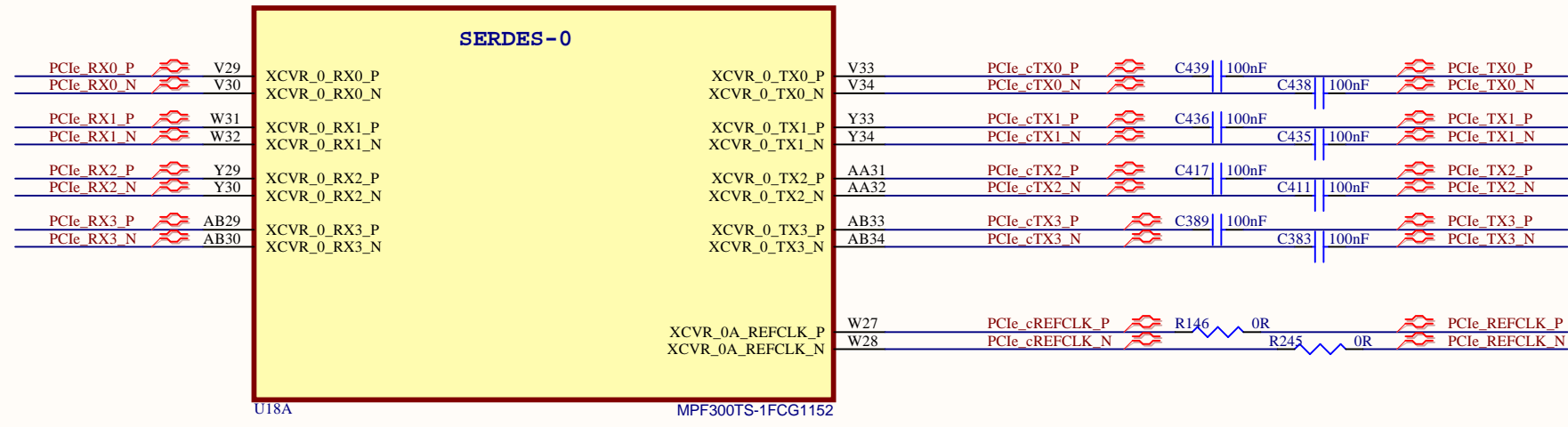
M9
Power Adapter
CP4A - Netzsteckeradapter, Euro, US, 3 A, Schwarz

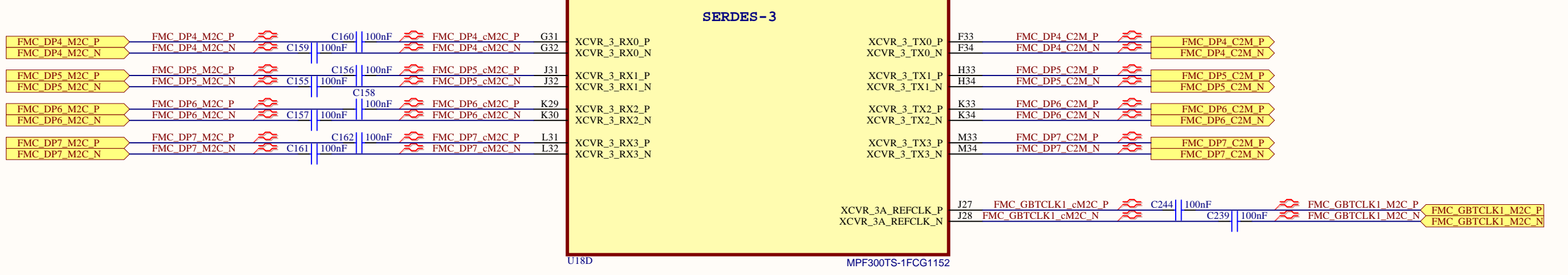
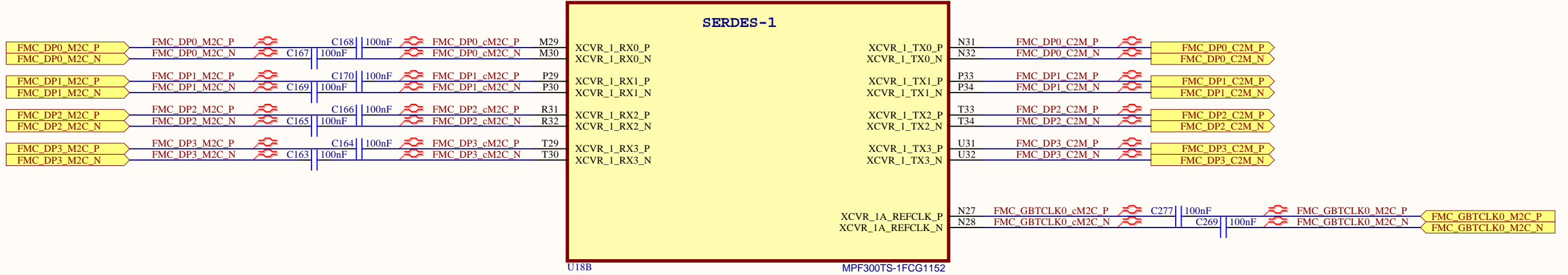
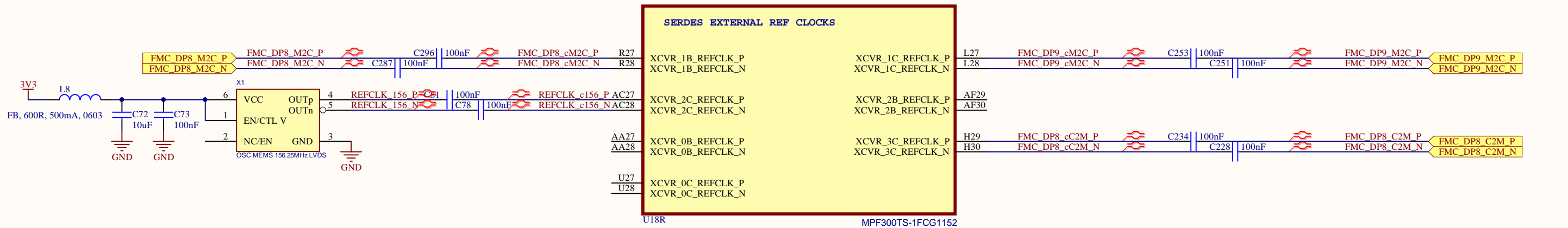
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Board package
Board package

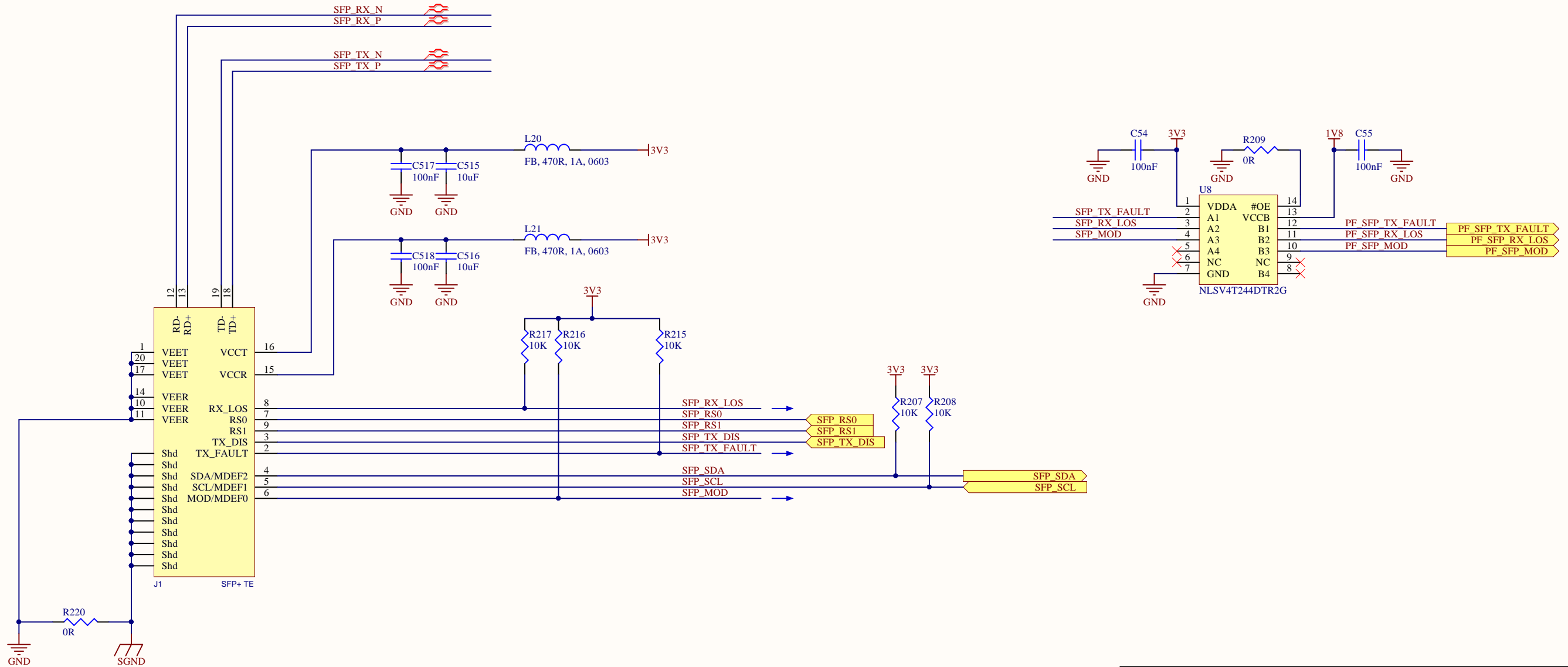
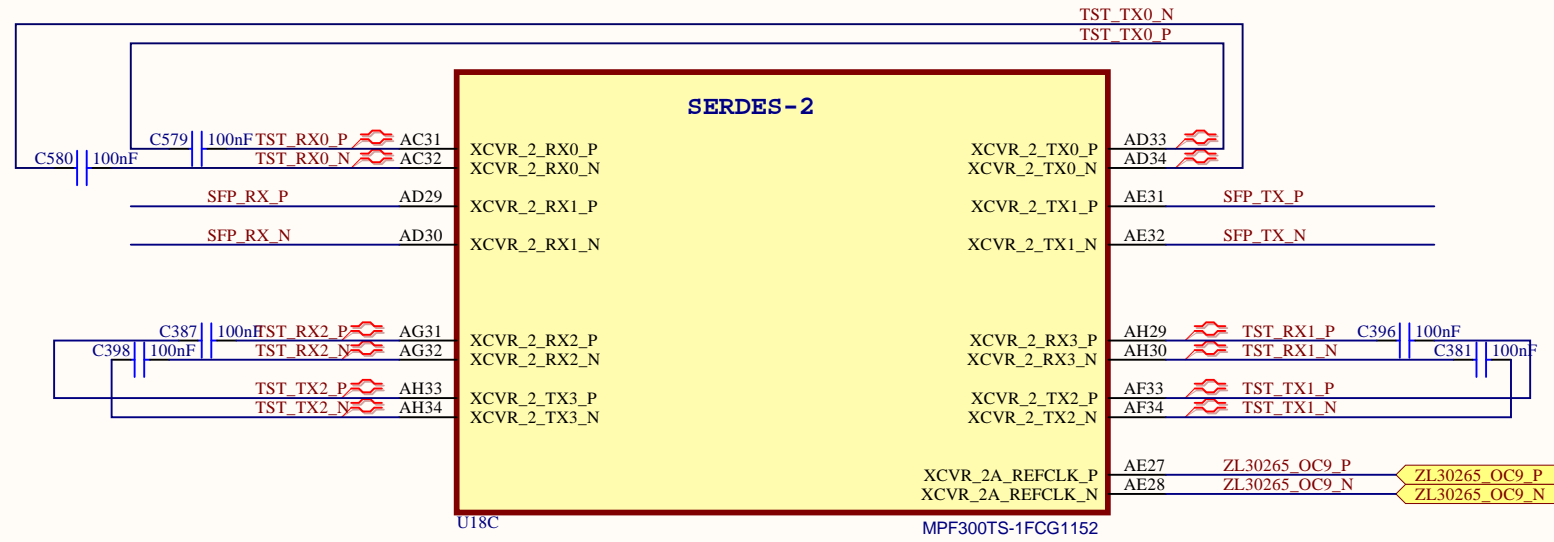
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Package Label
Package Label

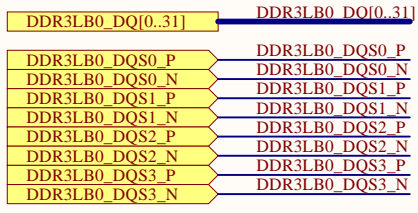
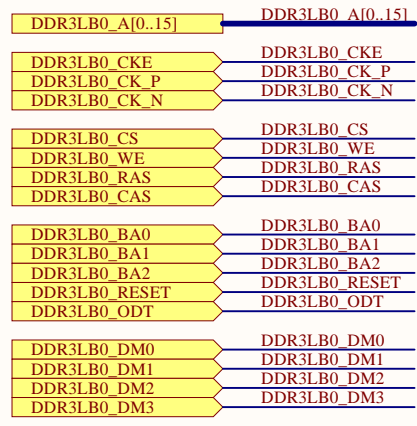
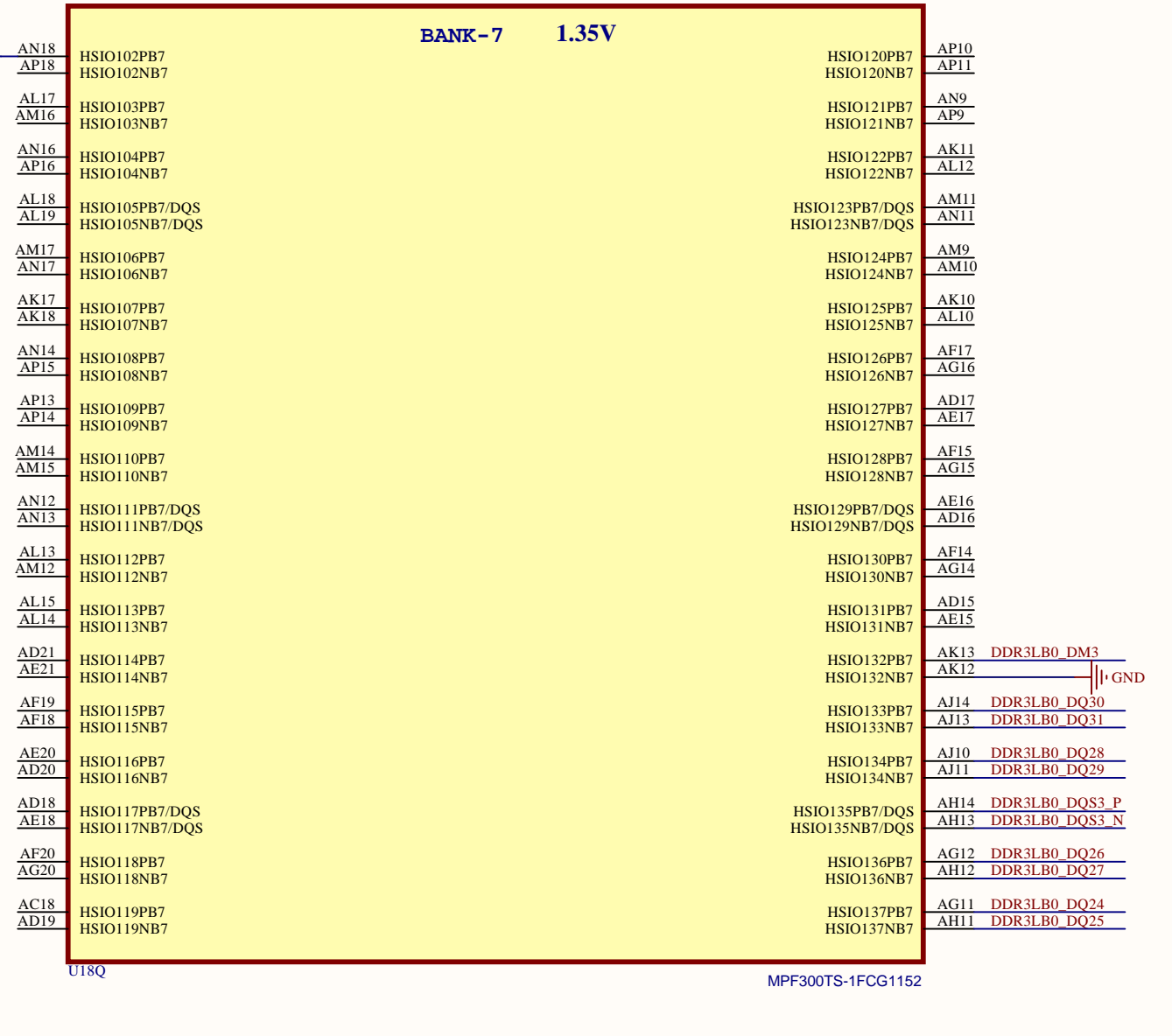
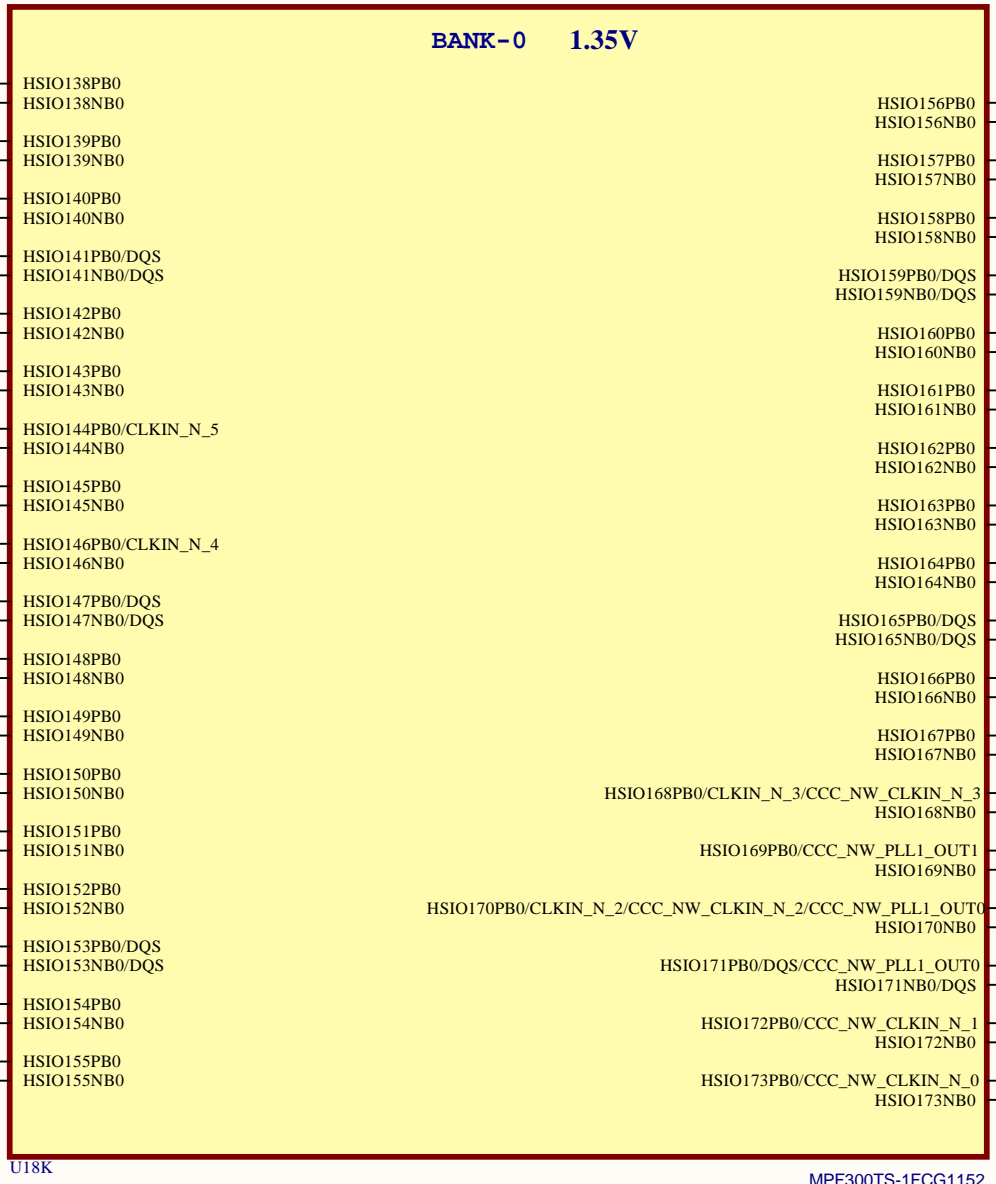
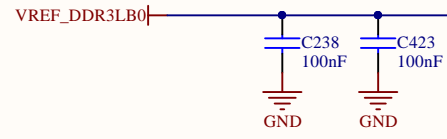
M12
Paper / License
Instruction paper / License

Project: ARROW Polarfire Everest Development Board	Revision: B	
Board: EVEREST-DEV-BOARD	Code: (-ES)	
Description: Microsemi PolarFire FPGA Dev Kit	Date: 03.12.2018	
File: Accessories-Rev.B.SchDoc	Sheet 0 of 37	









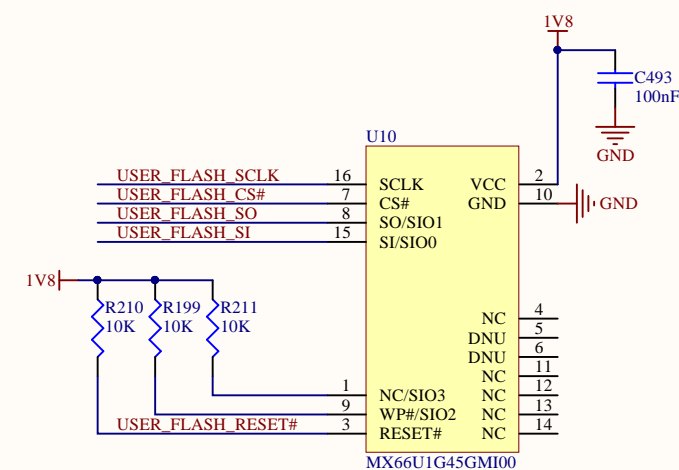
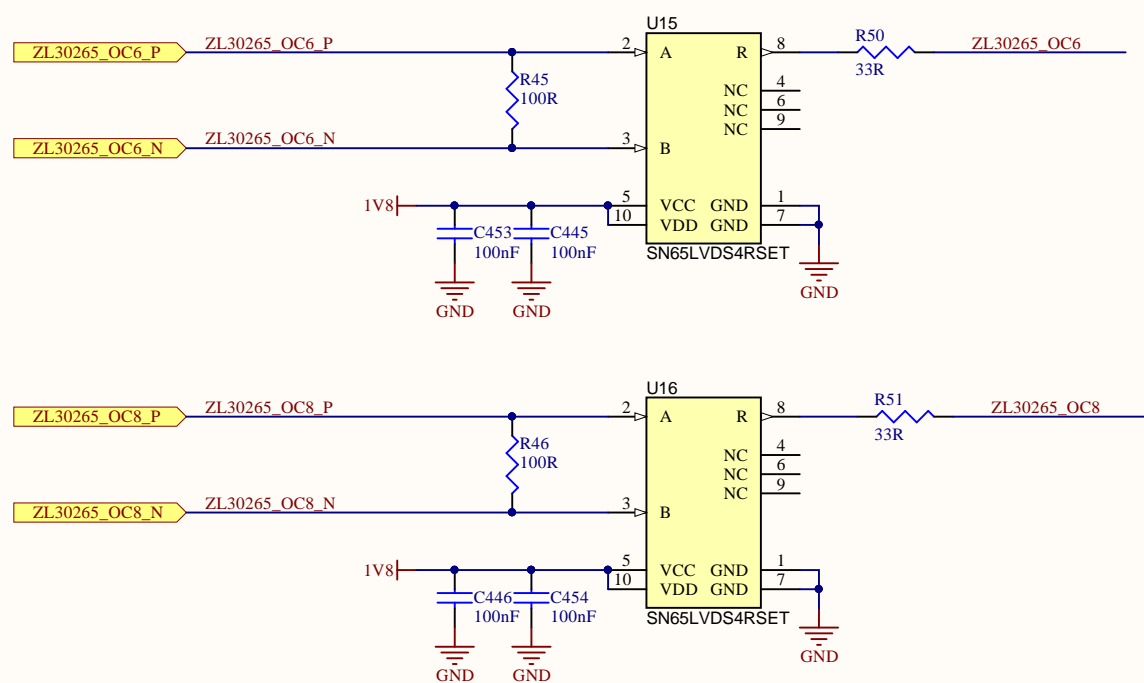
HDMI_TX_D[0..23] HDMI_TX_D[0..23]

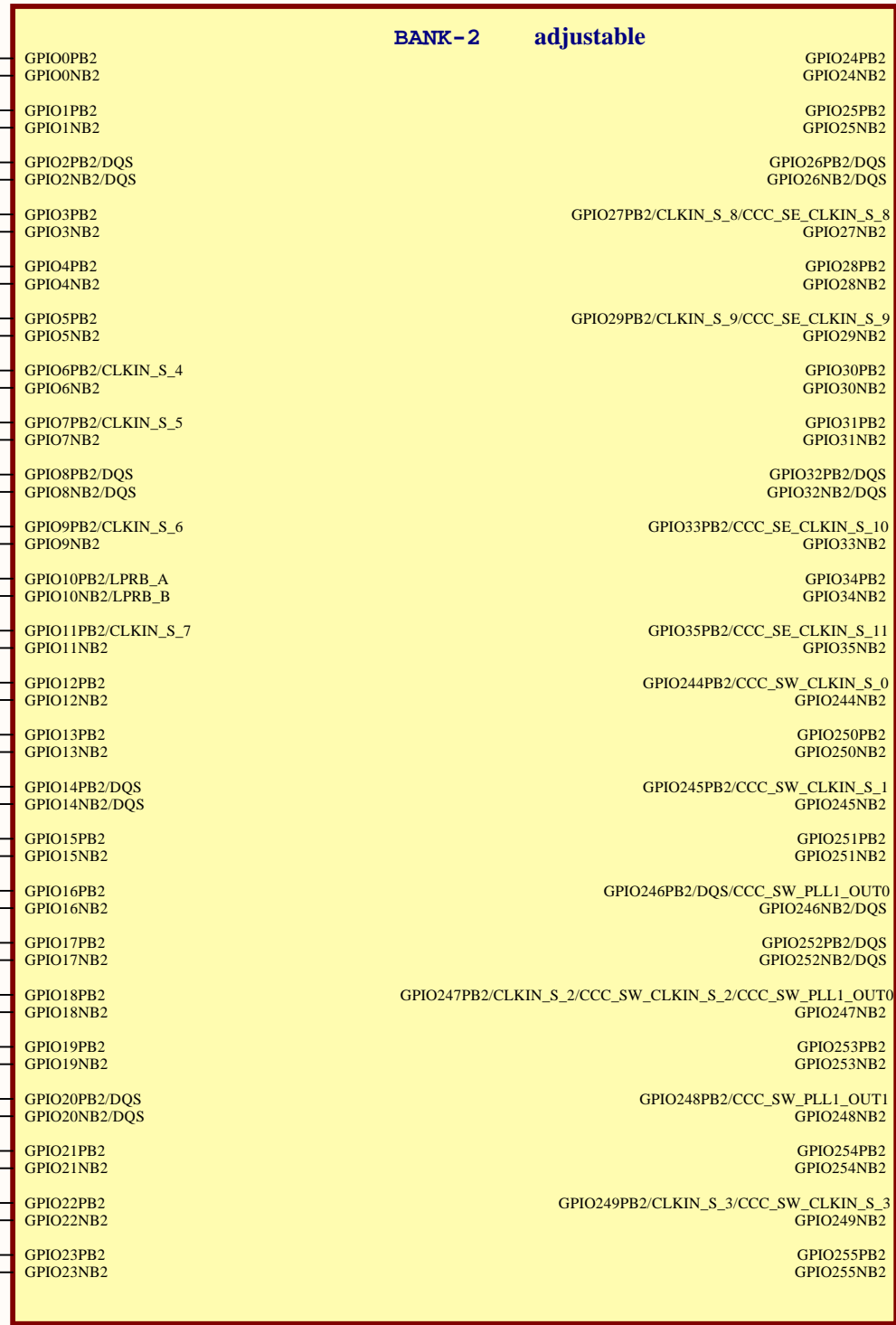
BANK-1 1.8V



U18L

MPF300TS-1FCG1152





U18M MPF300TS-1FCG1152

Project: ARROW Polarfire Everest Development Board	Revision: B
Board: EVEREST-DEV-BOARD	Code: (-ES)
Description: Microsemi PolarFire FPGA Dev Kit	Date: 03.12.2018
File: PF_Bank2_GPIO-Rev.B.SchDoc	Sheet 6 of 37

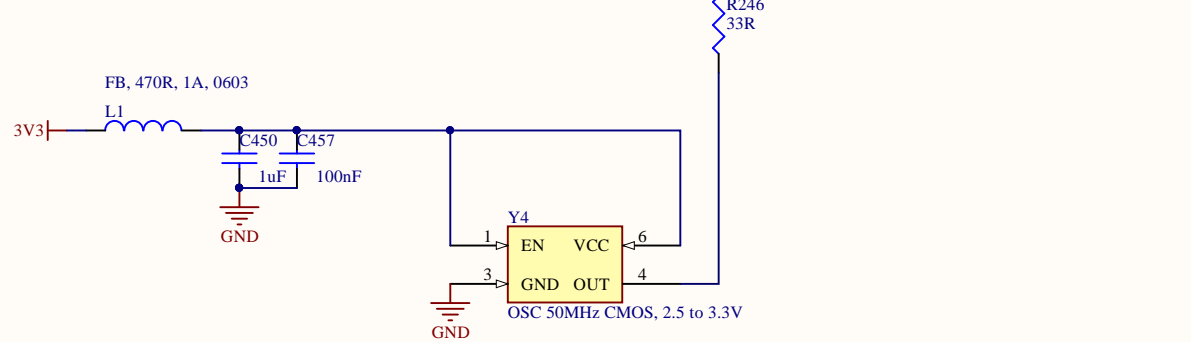
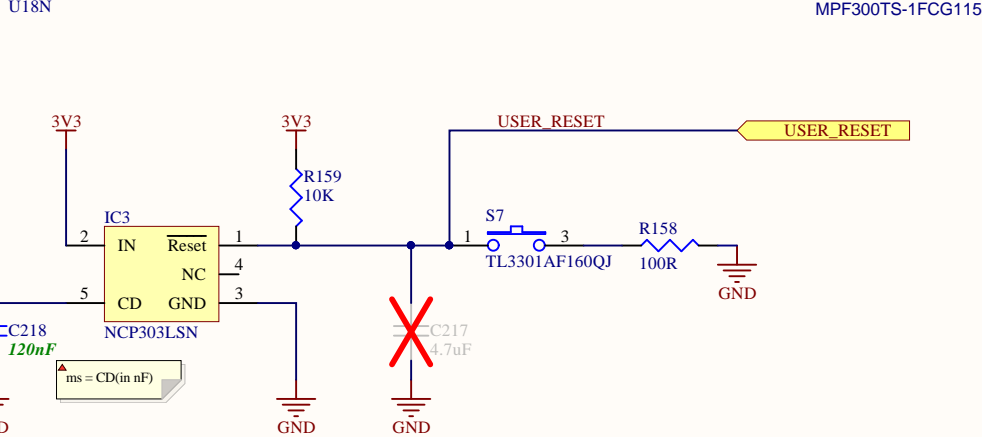
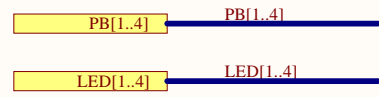


BANK-4 3.3V

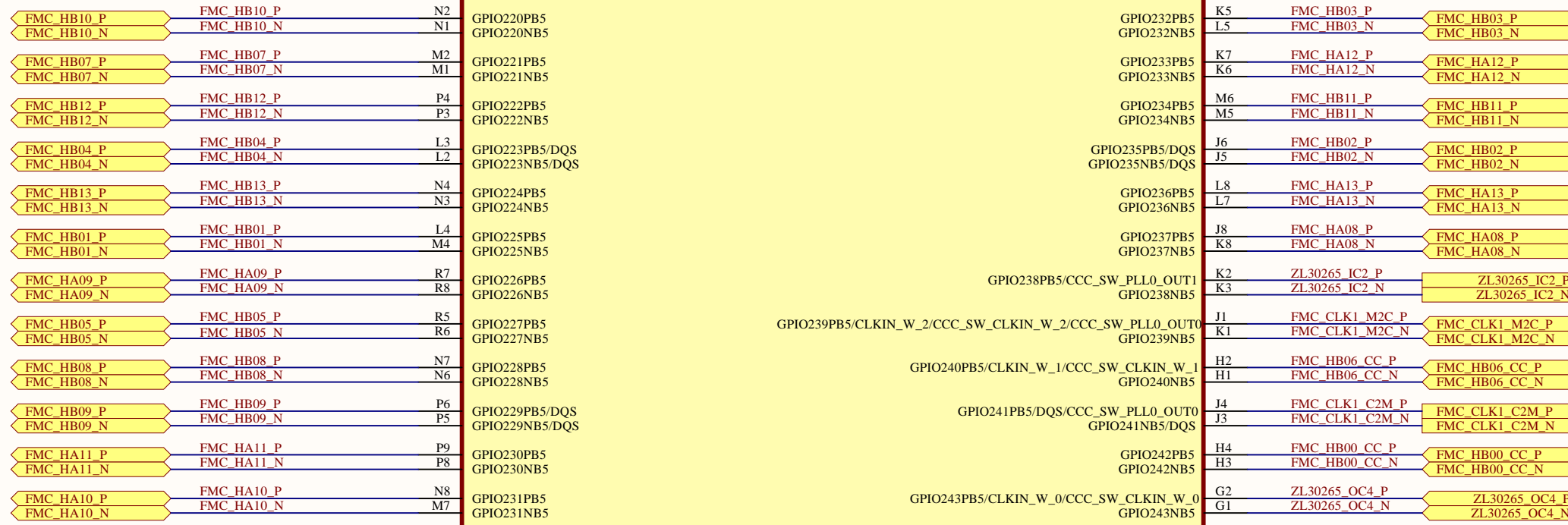
SFP_SDA	SFP_SDA	AC2
SFP_RS0	SFP_RS0	AD3
ZL30722_MOSI	ZL30722_MOSI	AC1
SFP_SCL	SFP_SCL	AD1
SGMII_RX2_P	SGMII_RX2_P	AB2
SGMII_RX2_N	SGMII_RX2_N	AB1
SGMII_TX2_P	SGMII_TX2_P	AB4
SGMII_TX2_N	SGMII_TX2_N	AC3
FASTLINKFAIL	FASTLINKFAIL	AC7
ZL30722_RSTn	ZL30722_RSTn	AC6
1588_LOAD_SAVE	1588_LOAD_SAVE	AB7
PMOD_IO08	PMOD_IO08	AB6
FPGA_1588REFCLK_P	FPGA_1588REFCLK_P	AD4
FPGA_1588REFCLK_N	FPGA_1588REFCLK_N	AD5
1588_SPI_SCLK	1588_SPI_SCLK	AC9
VSC8575_SPI_CS	VSC8575_SPI_CS	AC8
PMOD_IO02	PMOD_IO02	AB5
PCle_PRSN_T	PCle_PRSN_T 0R R238	AC4
ZL30722_CS_n	ZL30722_CS_n	AB9
SFP_RS1	SFP_RS1	AA8
VSC8575_MDC	VSC8575_MDC	AC11
VSC8575_MDIO	VSC8575_MDIO	AC12
ZL30722_MISO	ZL30722_MISO	AB14
VSC8575_MDINT	VSC8575_MDINT	AC13
VSC8575_COMA_MODE	VSC8575_COMA_MODE	AB11
CLK_SQUELCH_IN	CLK_SQUELCH_IN	AB10
VSC8575_NRESET	VSC8575_NRESET	AB12
VSC8575_SPI_DI	VSC8575_SPI_DI	AA12
FMC_PRSN_T_M2C	FMC_PRSN_T_M2C	AA14
ZL30722_SCLK	ZL30722_SCLK	AA13
1588_SPI_DO	1588_SPI_DO	AA10
PF_UART1_TX	PF_UART1_TX	AA9
PMOD_IO01	PMOD_IO01	AA3
VSC8575_SPI_DO	VSC8575_SPI_DO	AA2
PMOD_IO07	PMOD_IO07	AA4
PMOD_IO03	PMOD_IO03	AA5
SGMII_RX1_P	SGMII_RX1_P	Y3
SGMII_RX1_N	SGMII_RX1_N	Y2
PMOD_IO04	PMOD_IO04	W4
ZL30265_RSTn	ZL30265_RSTn	W3
SGMII_TX1_P	SGMII_TX1_P	W1
SGMII_TX1_N	SGMII_TX1_N	Y1
PF_UART1_RX	PF_UART1_RX	W5
ZL30265_AC2	ZL30265_AC2	Y5
ZL30265_MOSI	ZL30265_MOSI	Y7
1588_PPS_0	1588_PPS_0	AA7

GPIO174PB4/CLKIN_W_7/CCC_NW_CLKIN_W_7/CCC_NW_PLL0_OUT0	GPIO174NB4
GPIO175PB4/DQS	GPIO175NB4/DQS
GPIO176PB4	GPIO176NB4
GPIO177PB4	GPIO177NB4
GPIO178PB4	GPIO178NB4
GPIO179PB4	GPIO179NB4
GPIO180PB4/CLKIN_W_6/CCC_NW_CLKIN_W_6/CCC_NW_PLL0_OUT1	GPIO180NB4
GPIO181PB4/DQS/CCC_NW_PLL0_OUT0	GPIO181NB4/DQS
GPIO182PB4	GPIO182NB4
GPIO183PB4	GPIO183NB4
GPIO184PB4	GPIO184NB4
GPIO185PB4	GPIO185NB4
GPIO186PB4	GPIO186NB4
GPIO187PB4/DQS	GPIO187NB4/DQS
GPIO188PB4	GPIO188NB4
GPIO189PB4	GPIO189NB4
GPIO190PB4	GPIO190NB4
GPIO191PB4	GPIO191NB4
GPIO192PB4	GPIO192NB4
GPIO193PB4/DQS	GPIO193NB4/DQS
GPIO194PB4	GPIO194NB4
GPIO195PB4	GPIO195NB4
GPIO196PB4	GPIO196NB4
GPIO197PB4	GPIO197NB4
GPIO198PB4	GPIO198NB4
GPIO199PB4/DQS	GPIO199NB4/DQS
GPIO200PB4	GPIO200NB4
GPIO201PB4	GPIO201NB4
GPIO202PB4	GPIO202NB4
GPIO203PB4	GPIO203NB4
GPIO204PB4	GPIO204NB4
GPIO205PB4/DQS	GPIO205NB4/DQS
GPIO206PB4	GPIO206NB4
GPIO207PB4	GPIO207NB4
GPIO208PB4	GPIO208NB4
GPIO209PB4	GPIO209NB4
GPIO210PB4	GPIO210NB4
GPIO211PB4/DQS	GPIO211NB4/DQS
GPIO212PB4	GPIO212NB4
GPIO213PB4	GPIO213NB4
GPIO214PB4	GPIO214NB4
GPIO215PB4/CLKIN_W_5/CCC_NW_CLKIN_W_5	GPIO215NB4
GPIO216PB4/CLKIN_W_4/CCC_NW_CLKIN_W_4	GPIO216NB4
GPIO217PB4/DQS	GPIO217NB4/DQS
GPIO218PB4	GPIO218NB4
GPIO219PB4/CLKIN_W_3/CCC_SW_CLKIN_W_3	GPIO219NB4

W6	ZL30265_MISO	ZL30265_MISO
Y6	ZL30265_CS_n	ZL30265_CS_n
V8	PB3	
V7	ZL30265_SCLK	ZL30265_SCLK
W8	LED3	
Y8	PB2	
W10	PB4	
Y10	VSC8575_SPI_CLK	VSC8575_SPI_CLK
V9	PF_UART0_RX	PF_UART0_RX
W9	LED4	
W11	ZL30722_TEST	ZL30722_TEST
Y11	1588_SPI_CS	1588_SPI_CS
V13	ZL30265_AC1	ZL30265_AC1
W13	ZL30722_PPS2	ZL30722_PPS2
Y12	ZL30722_AC1	ZL30722_AC1
Y13	ZL30722_AC0	ZL30722_AC0
V12	ZL30265_AC0	ZL30265_AC0
V11	ZL30722_PPS1	ZL30722_PPS1
U12	ZL30265_TEST	ZL30265_TEST
U11	LED1	
V14	FMC_PG_C2M	FMC_PG_C2M
W14	FMC_PG_M2C	FMC_PG_M2C
V3	PMOD_IO09	PMOD_IO09
V4	PMOD_IO10	PMOD_IO10
T3	USER_RESET	
T2		
V1	SGMII_TX0_P	SGMII_TX0_P
V2	SGMII_TX0_N	SGMII_TX0_N
P1	SFP_TX_DIS	SFP_TX_DIS
R1		
U2	SGMII_RX0_P	SGMII_RX0_P
U1	SGMII_RX0_N	SGMII_RX0_N
R3	PCle_SMCLK	PCle_SMCLK
R2	PCle_SMDAT	PCle_SMDAT
U6	PCle_PERST	PCle_PERST
V6	PCle_WAKE	PCle_WAKE
U4	FPGA_ZL30722_REFCLK_P	FPGA_ZL30722_REFCLK_P
U5	FPGA_ZL30722_REFCLK_N	FPGA_ZL30722_REFCLK_N
U10	ZL30265_OC1A_P	ZL30265_OC1A_P
U9	ZL30265_OC1A_N	ZL30265_OC1A_N
T5	LED2	
T4	PB1	
T7	FMC_SCL	FMC_SCL
U7	PF_UART0_TX	PF_UART0_TX
T9		
T8	FMC_SDA	FMC_SDA

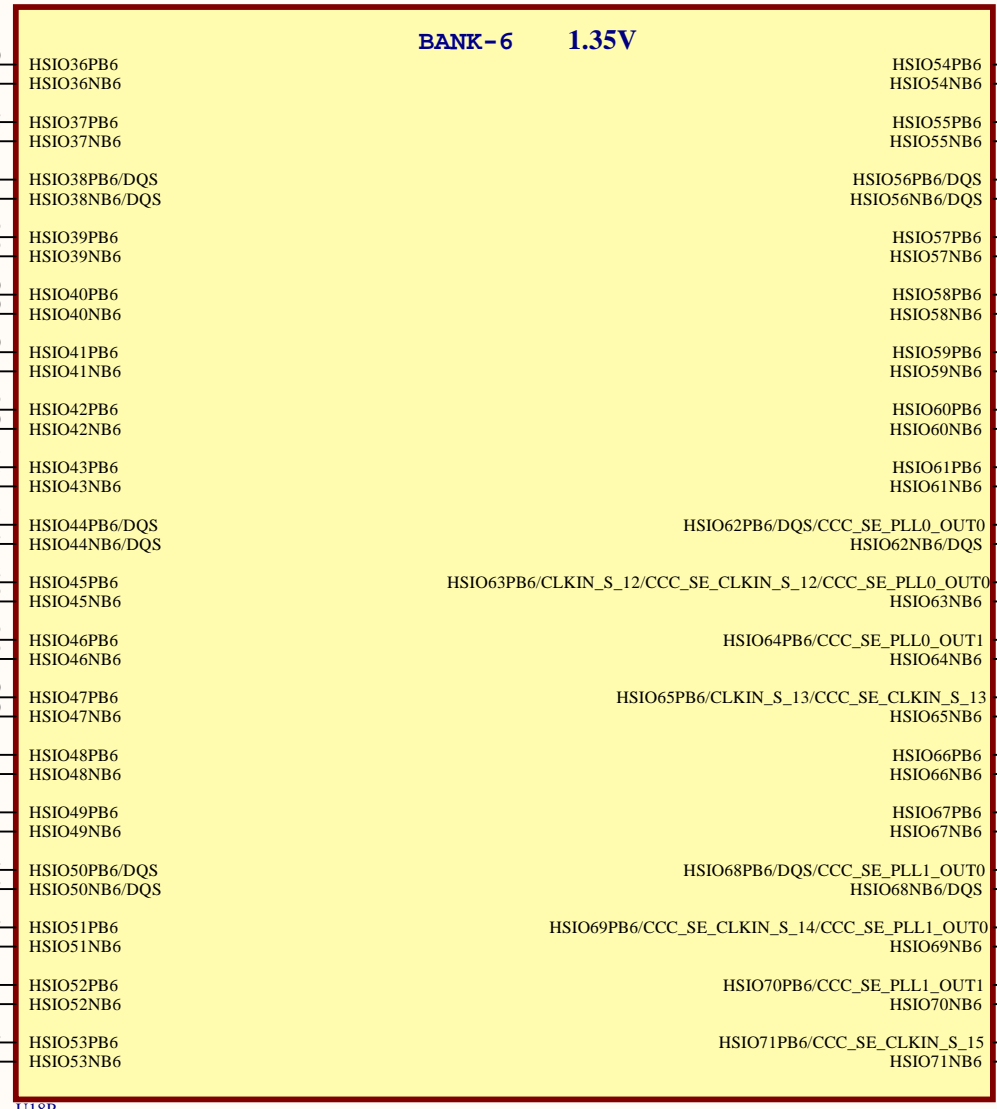
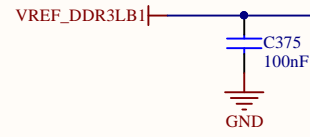


BANK-5 adjustable

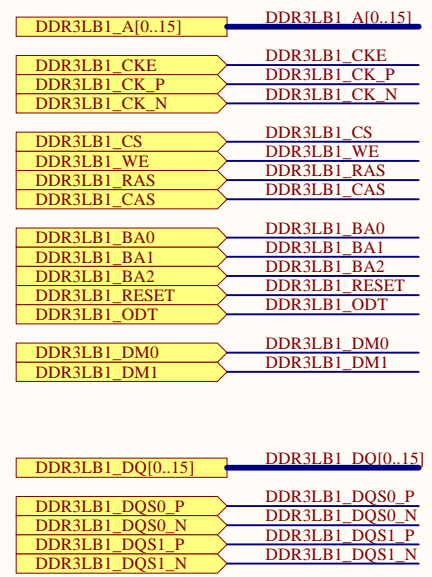


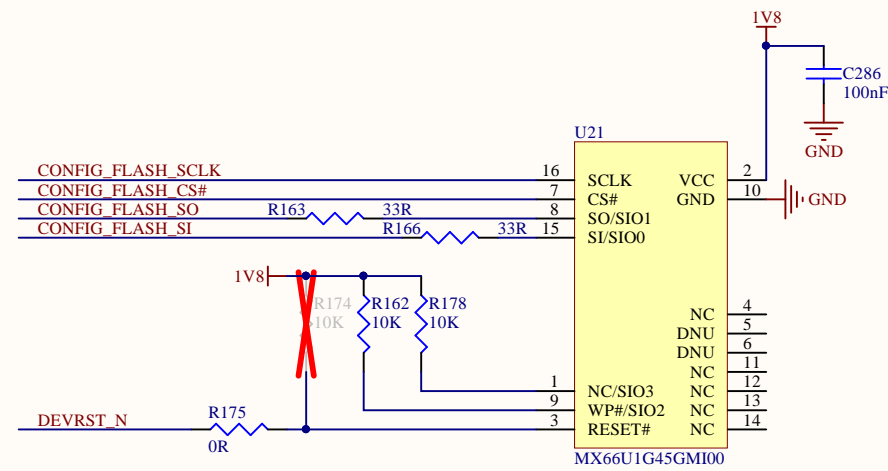
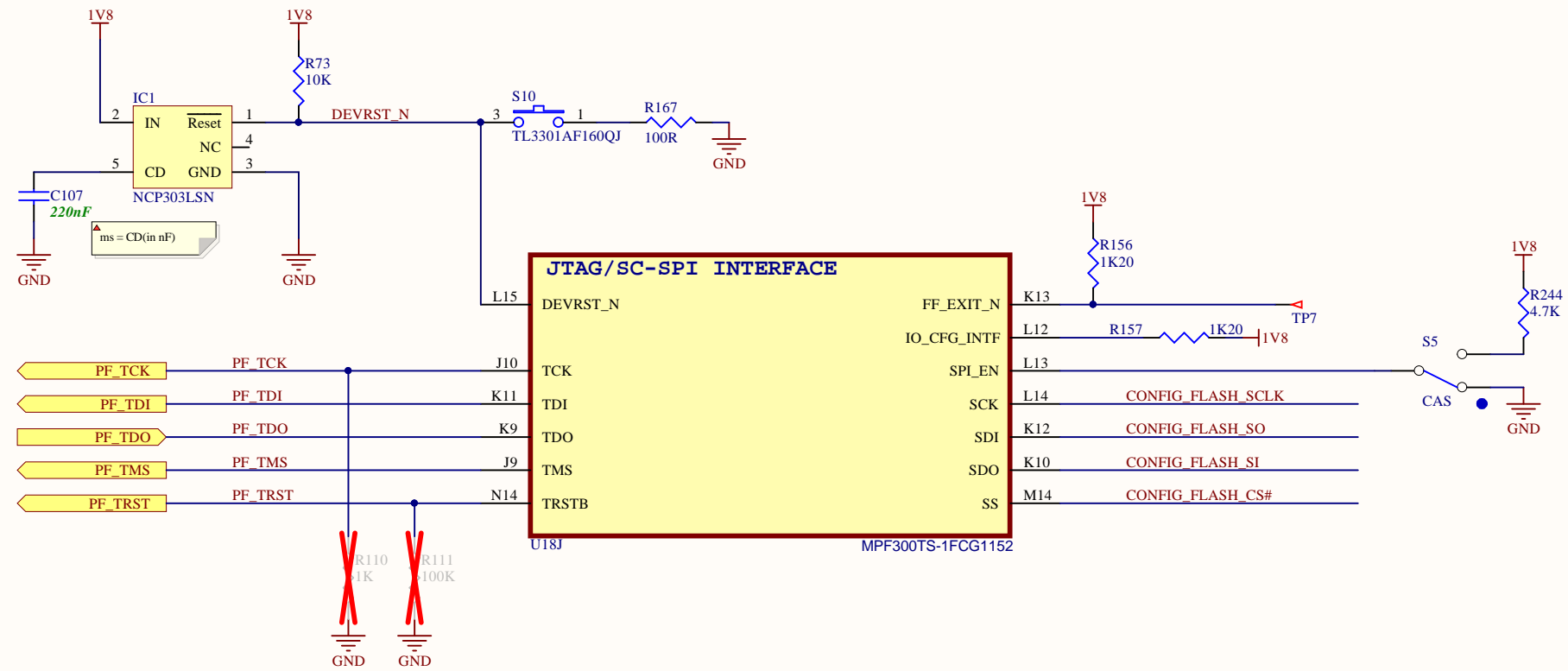
U180

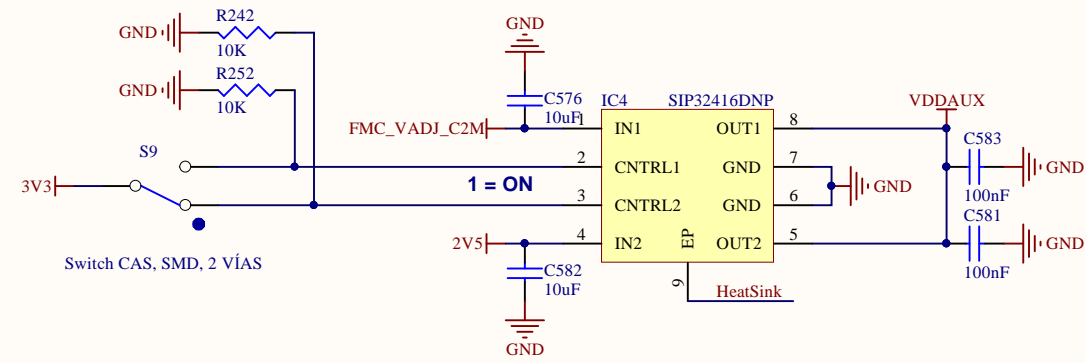
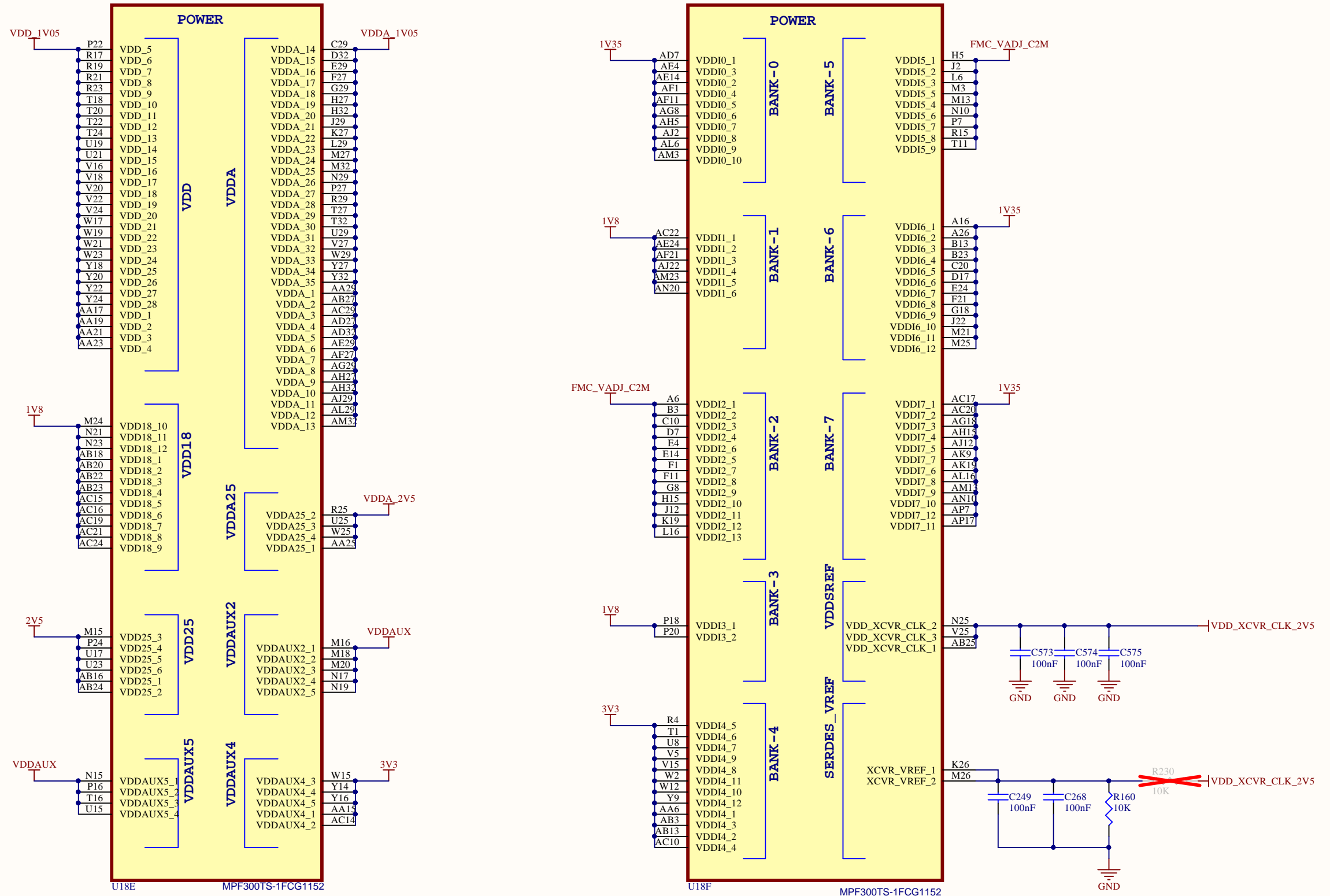
MPF300TS-1FCG1152



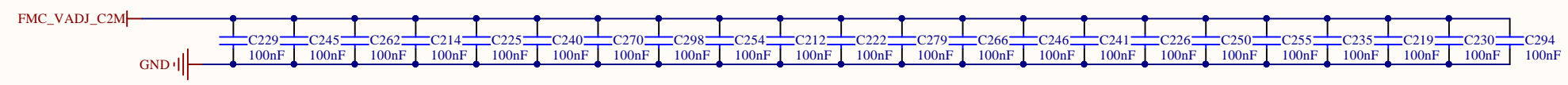
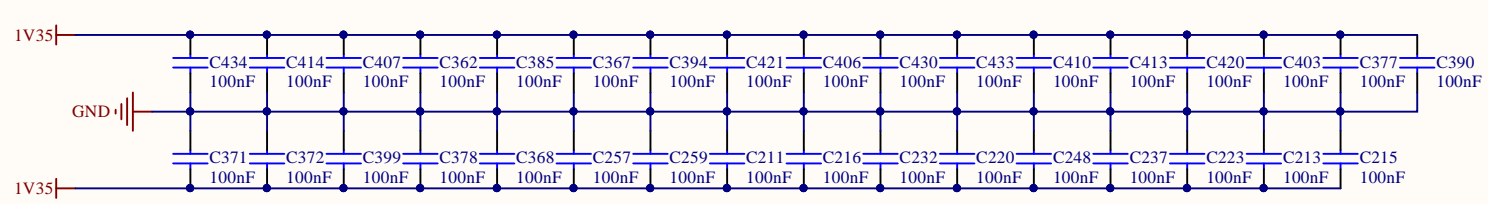
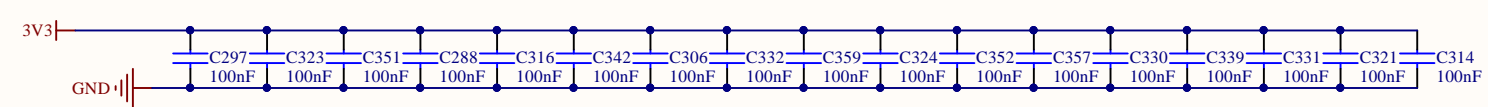
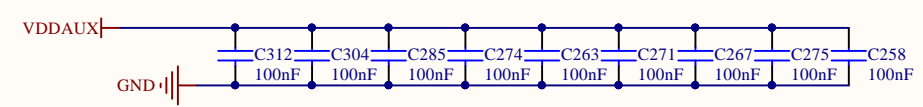
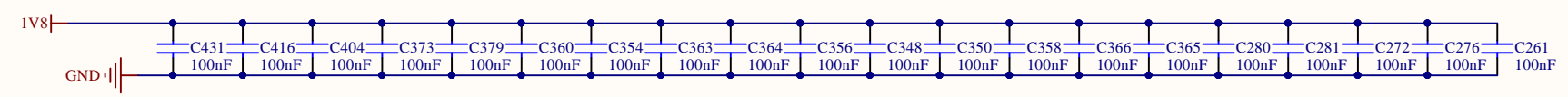
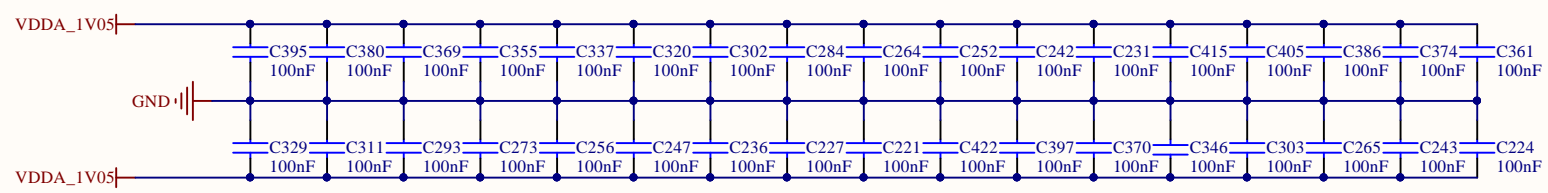
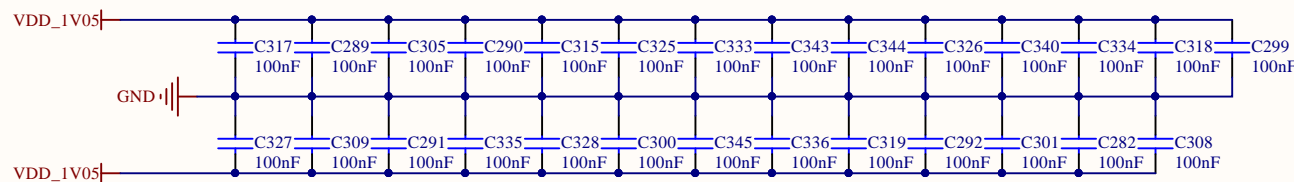
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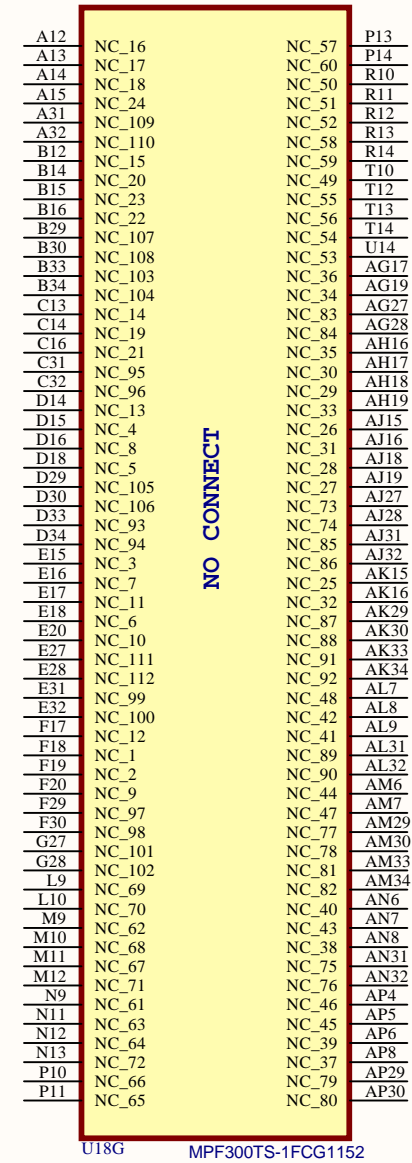
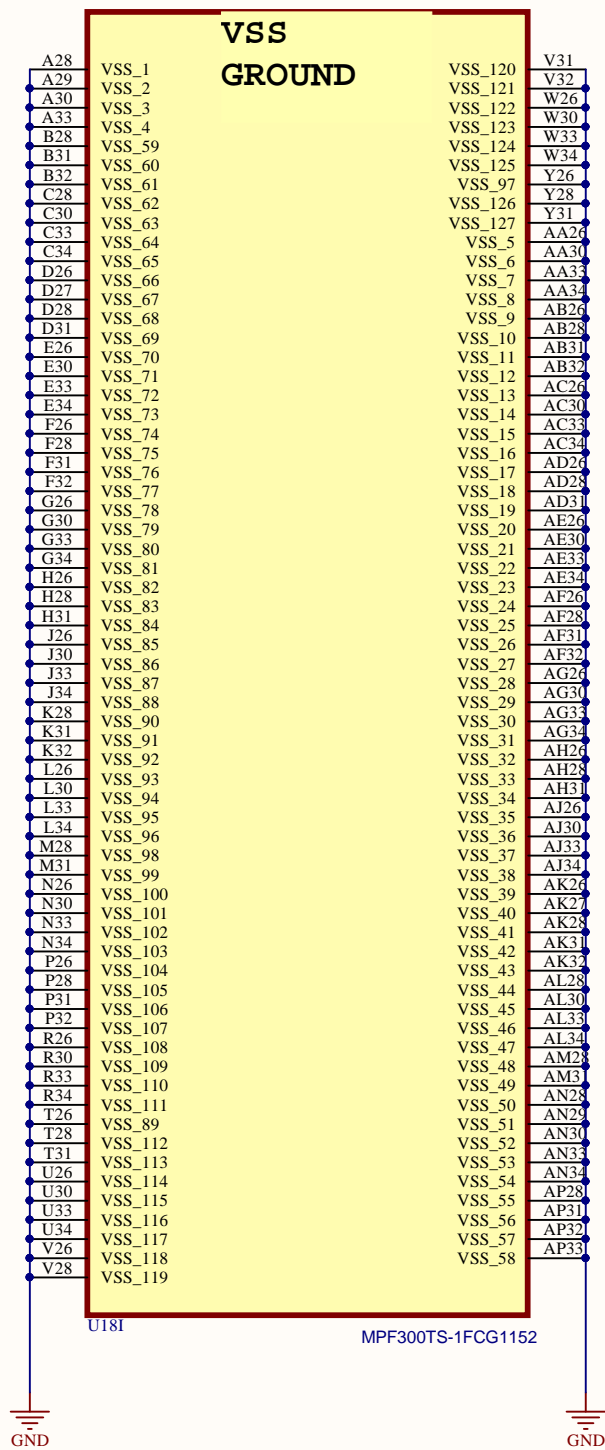
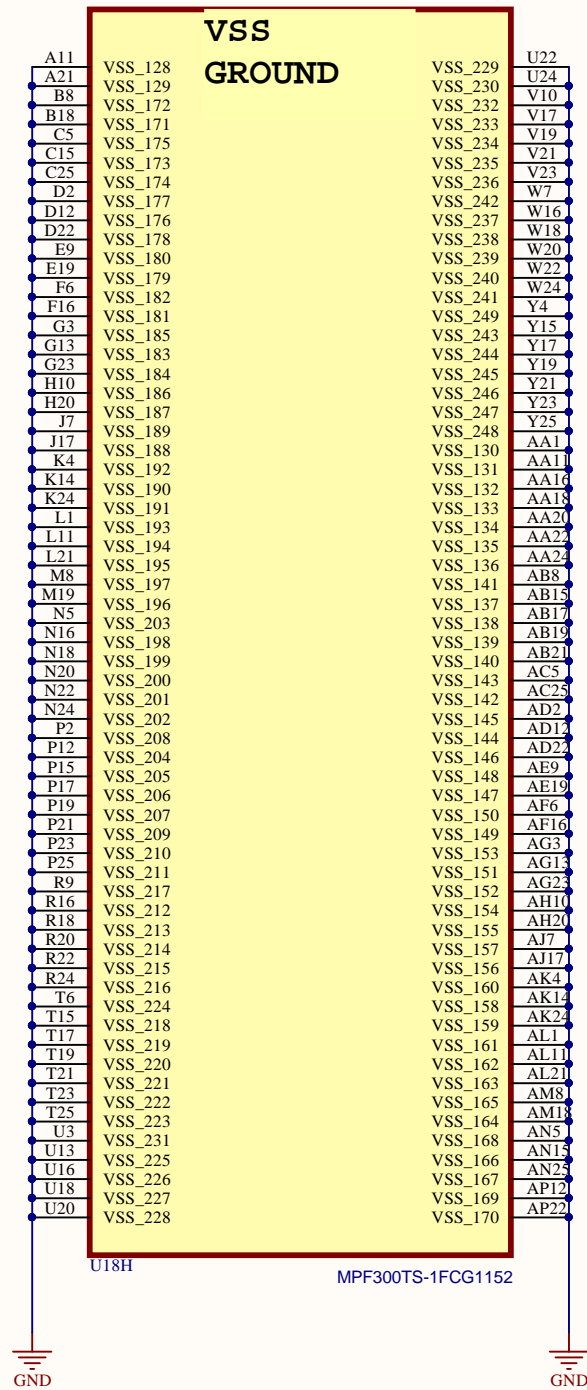


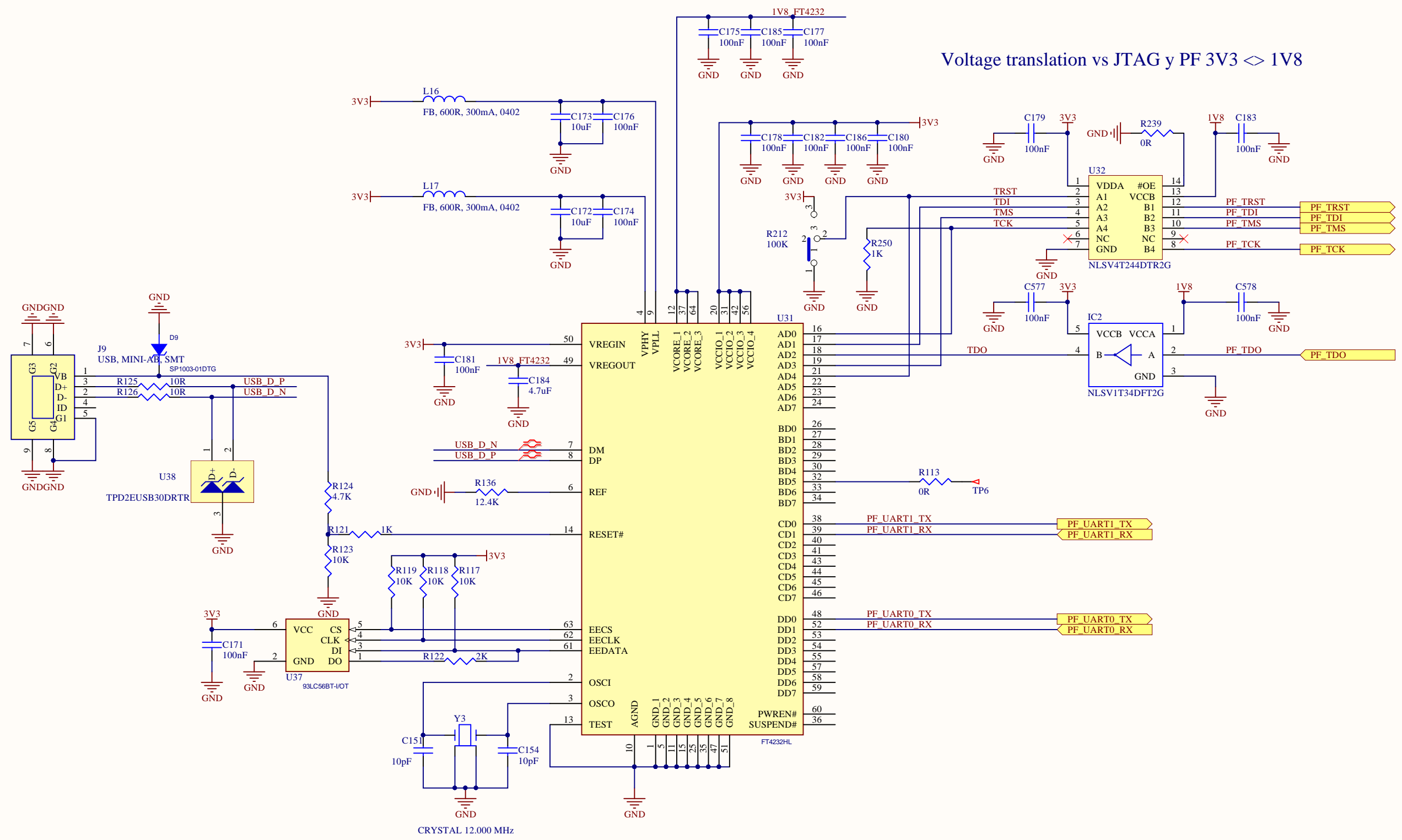




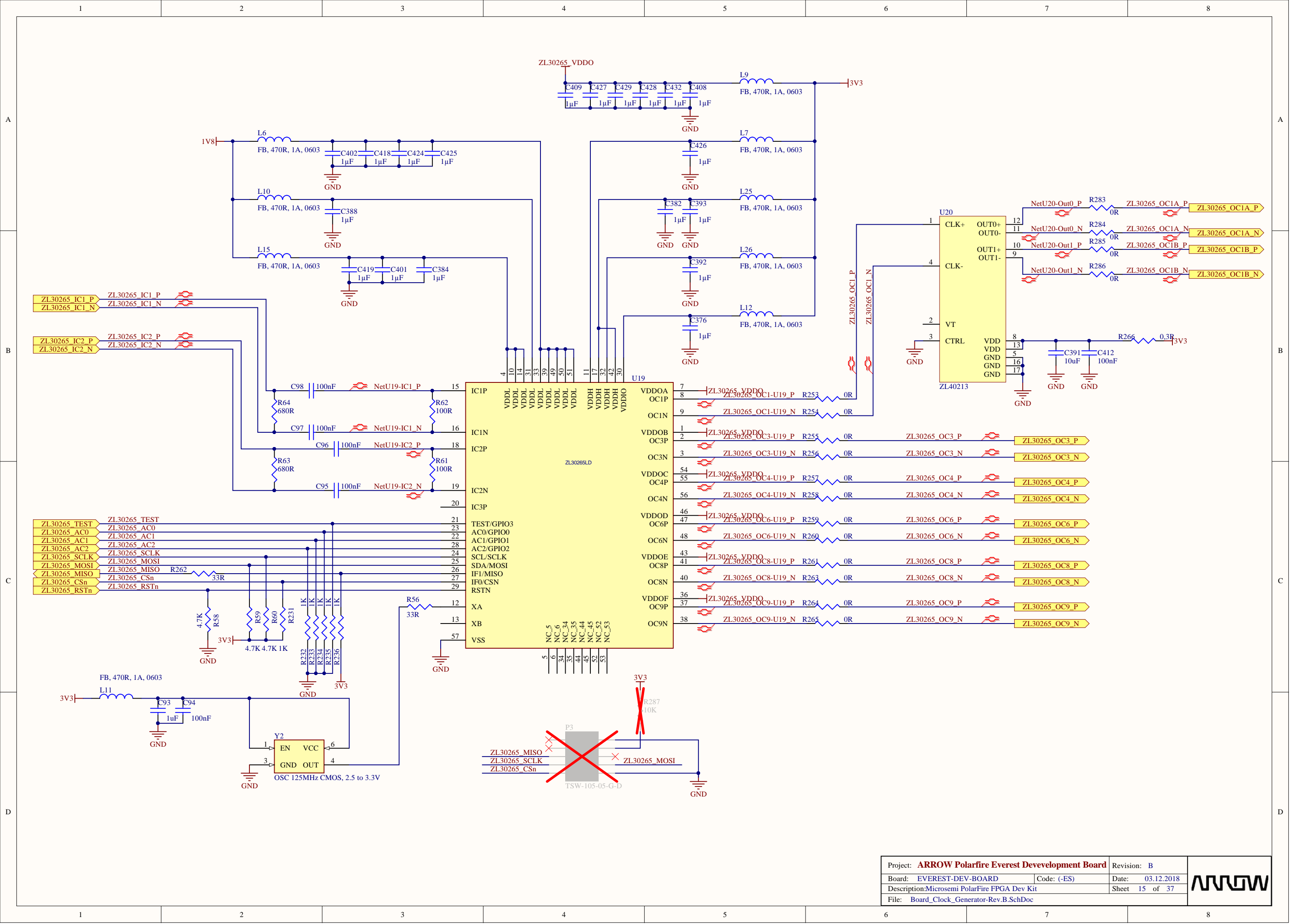
Project: ARROW Polarfire Everest Development Board	Revision: B	
Board: EVEREST-DEV-BOARD	Code: (-ES)	
Description: Microsemi PolarFire FPGA Dev Kit	Date: 03.12.2018	
File: PF_Power-Rev.B.SchDoc	Sheet 11 of 37	





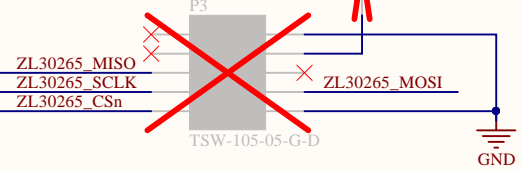
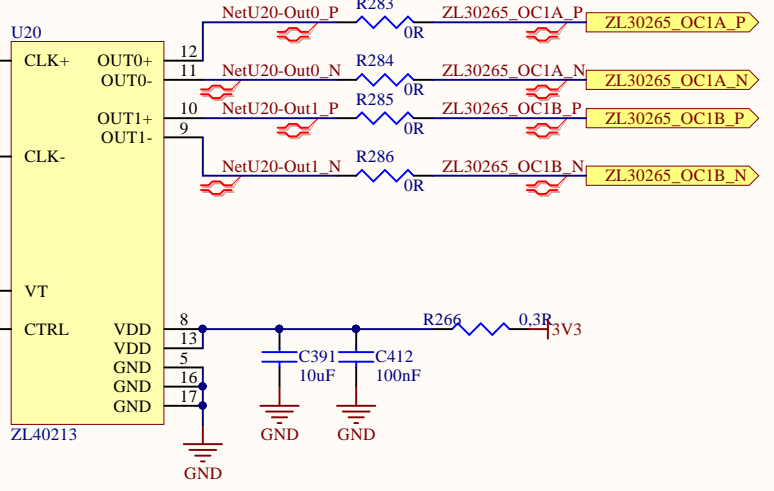
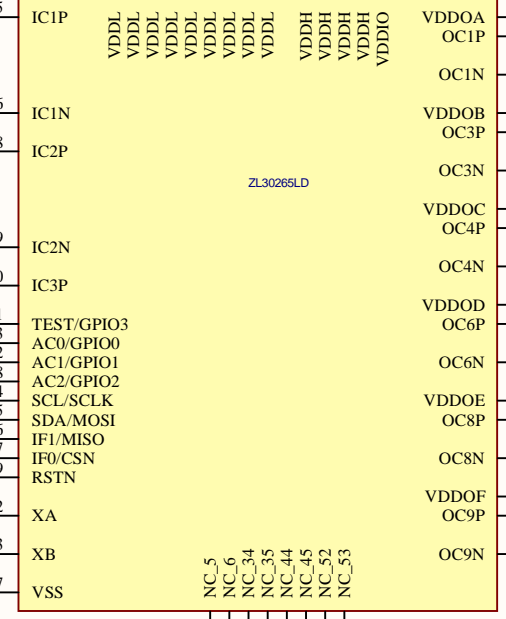


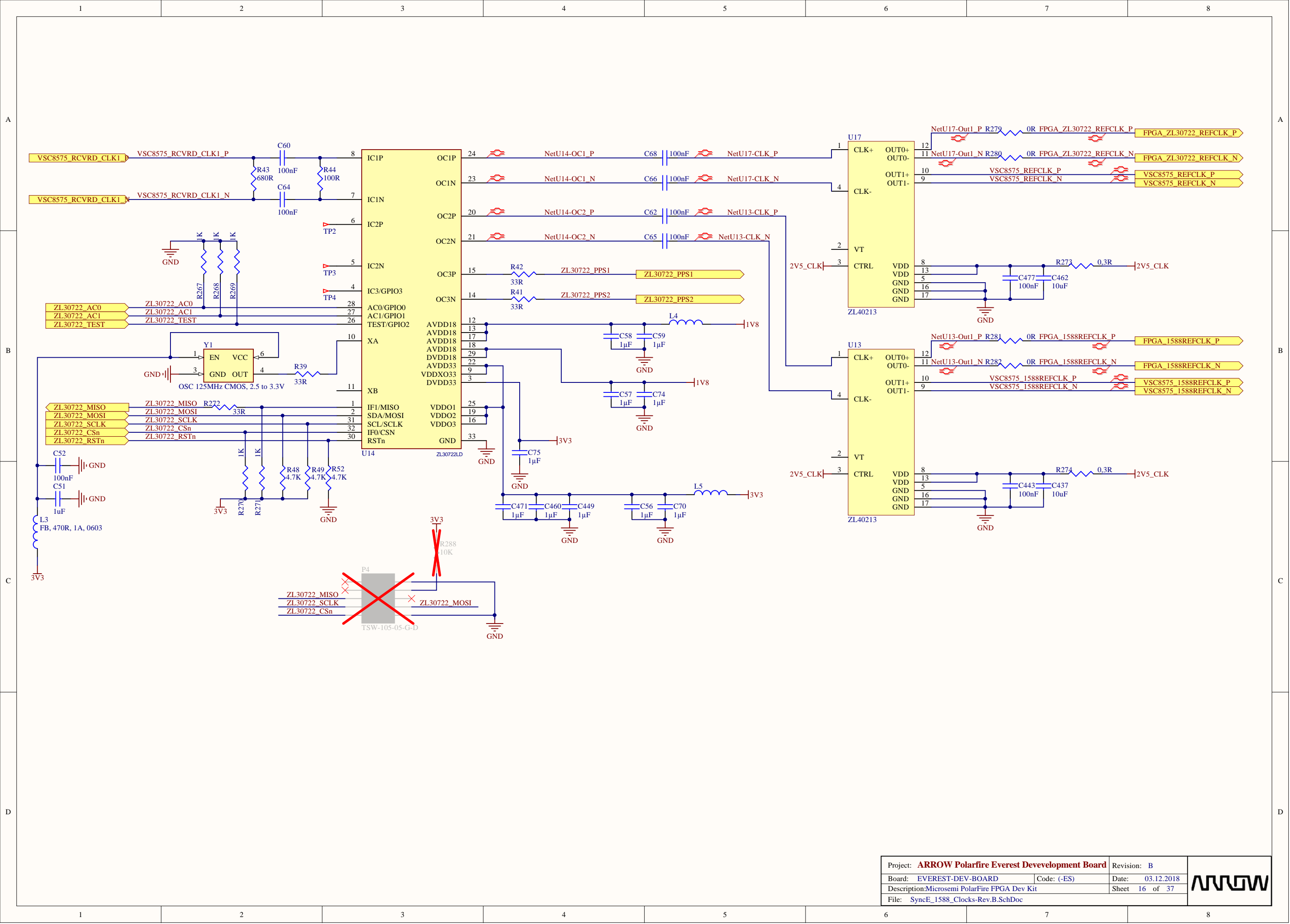
Voltage translation vs JTAG y PF 3V3 \leftrightarrow 1V8

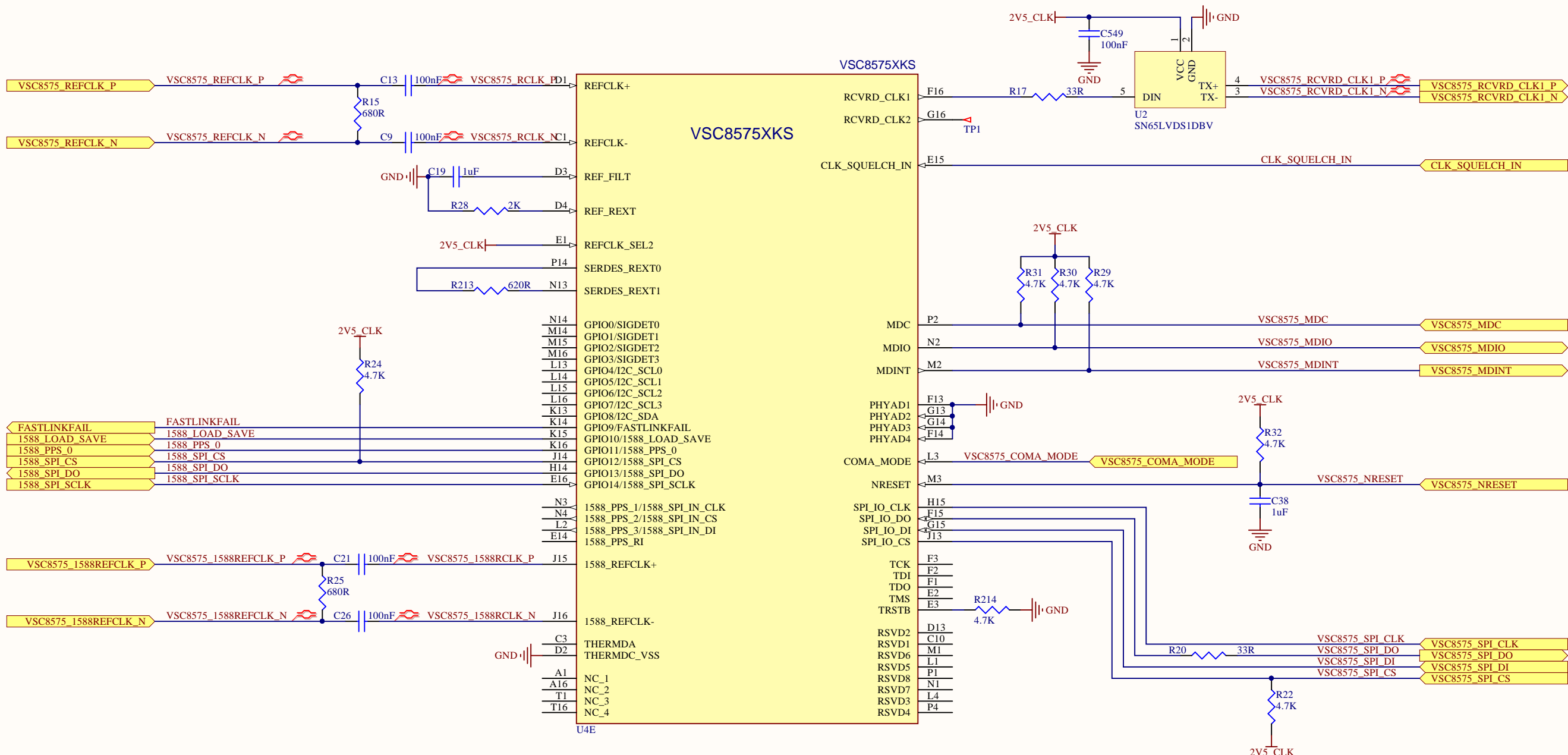


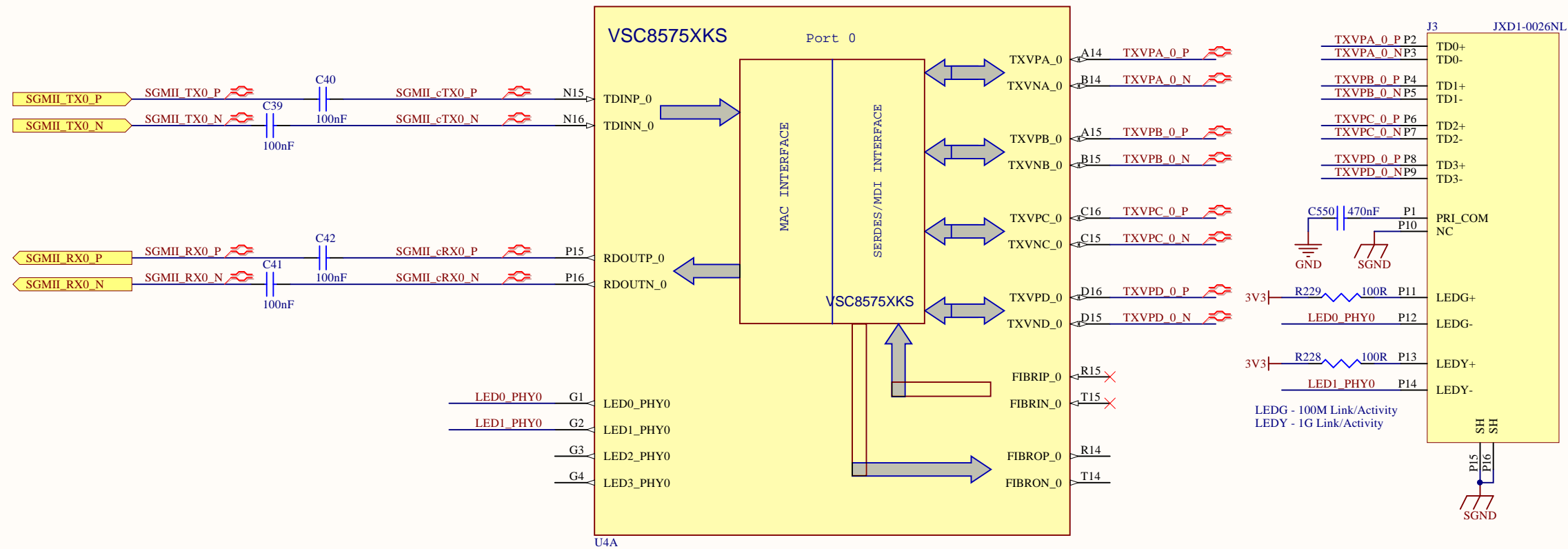
- ZL30265_IC1_P
- ZL30265_IC1_N
- ZL30265_IC2_P
- ZL30265_IC2_N

- ZL30265_TEST
- ZL30265_AC0
- ZL30265_AC1
- ZL30265_AC2
- ZL30265_SCLK
- ZL30265_MOSI
- ZL30265_MISO
- ZL30265_CS_n
- ZL30265_RST_n

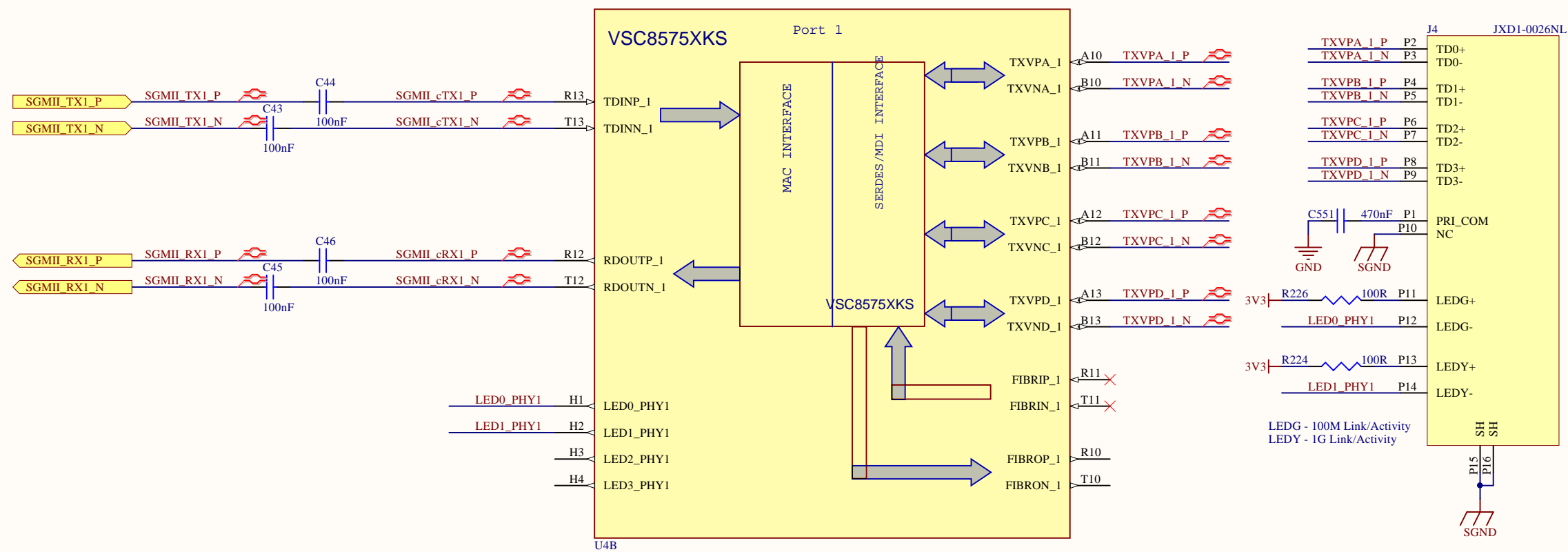




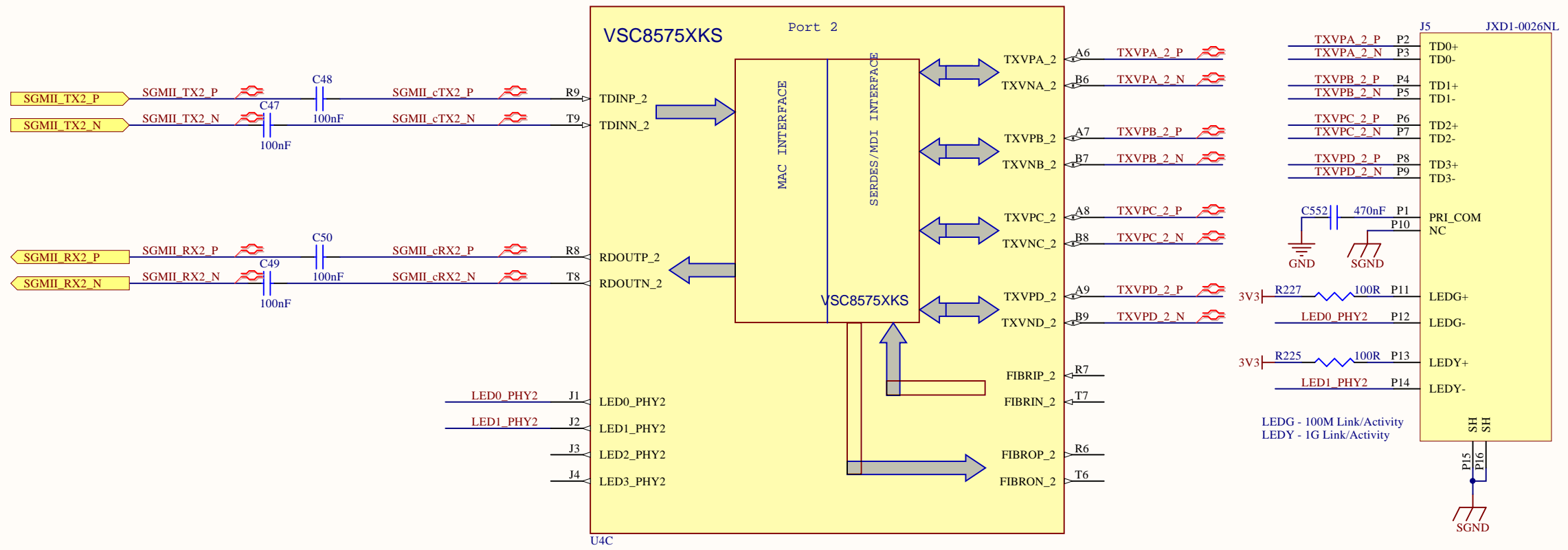


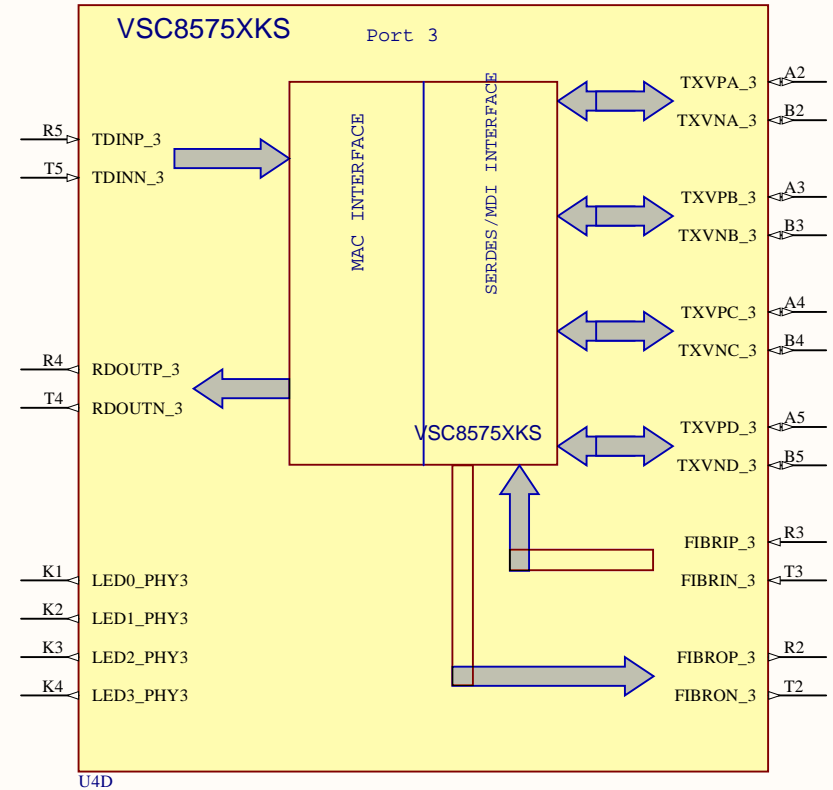


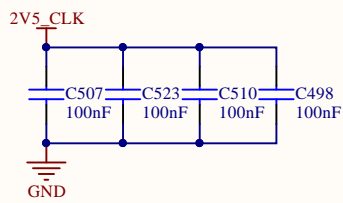
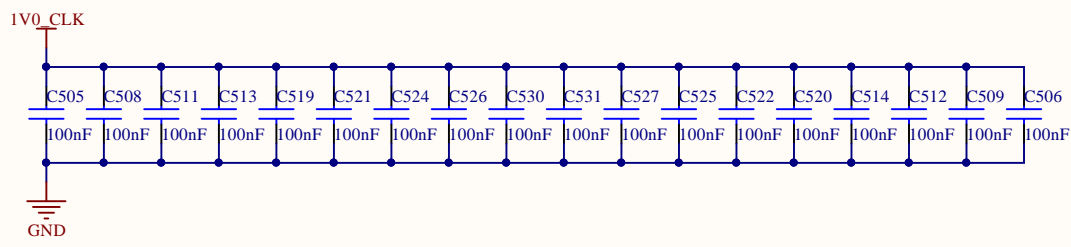
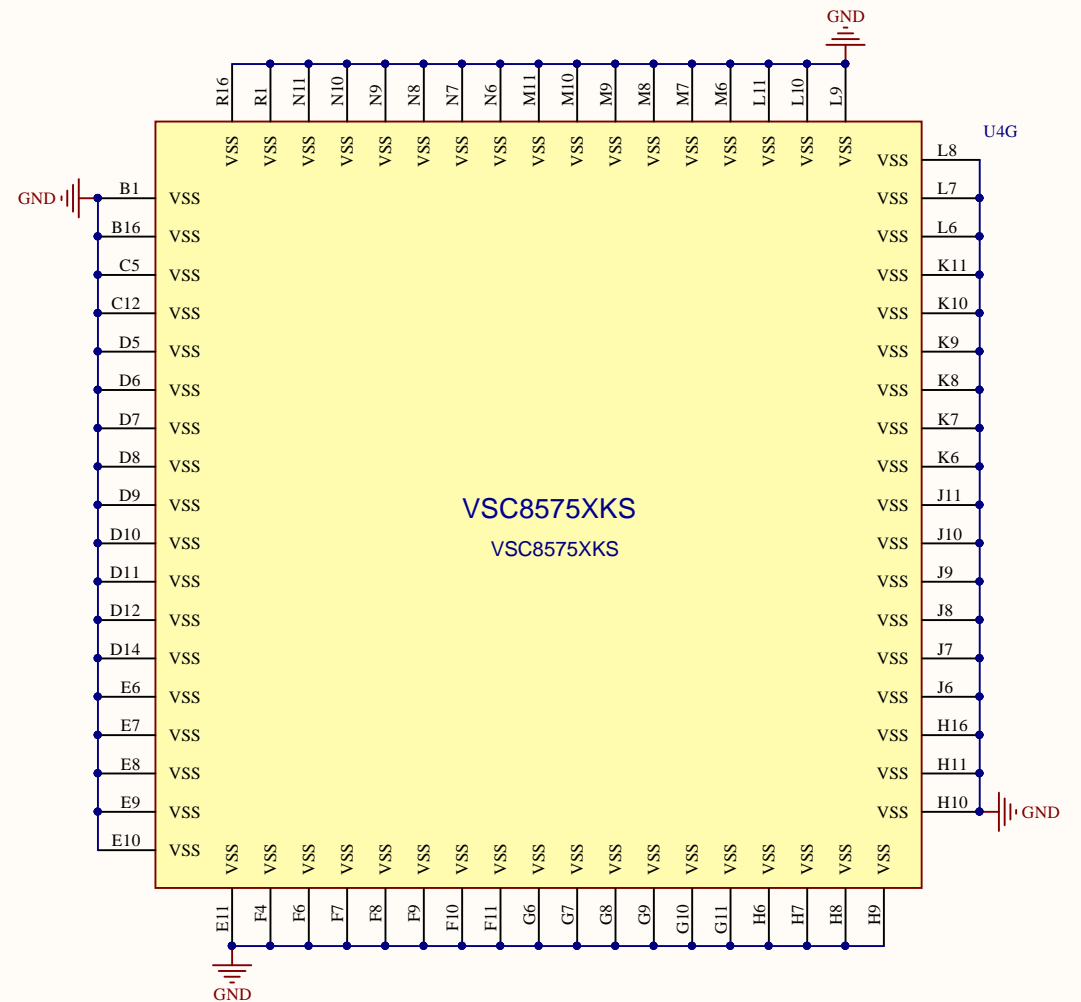
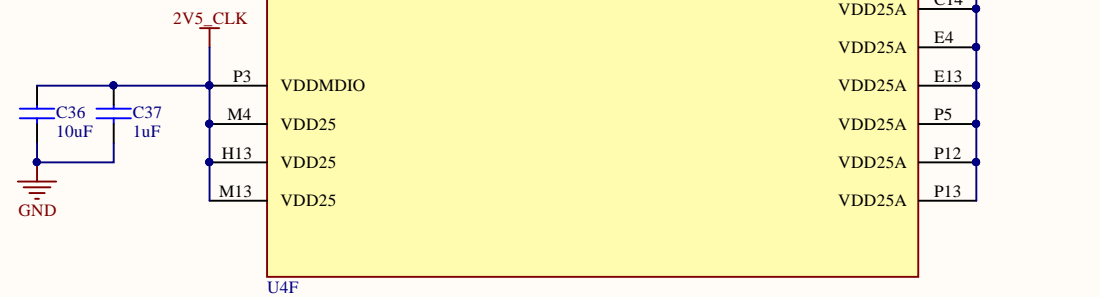
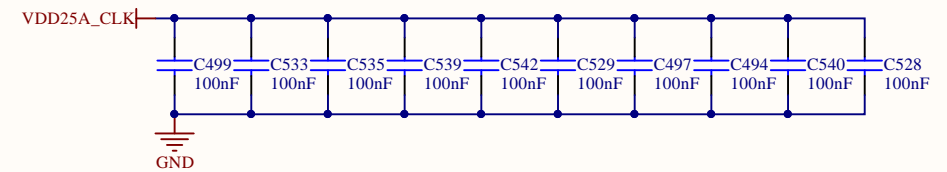
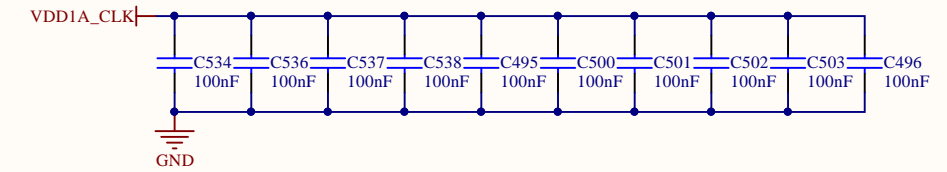
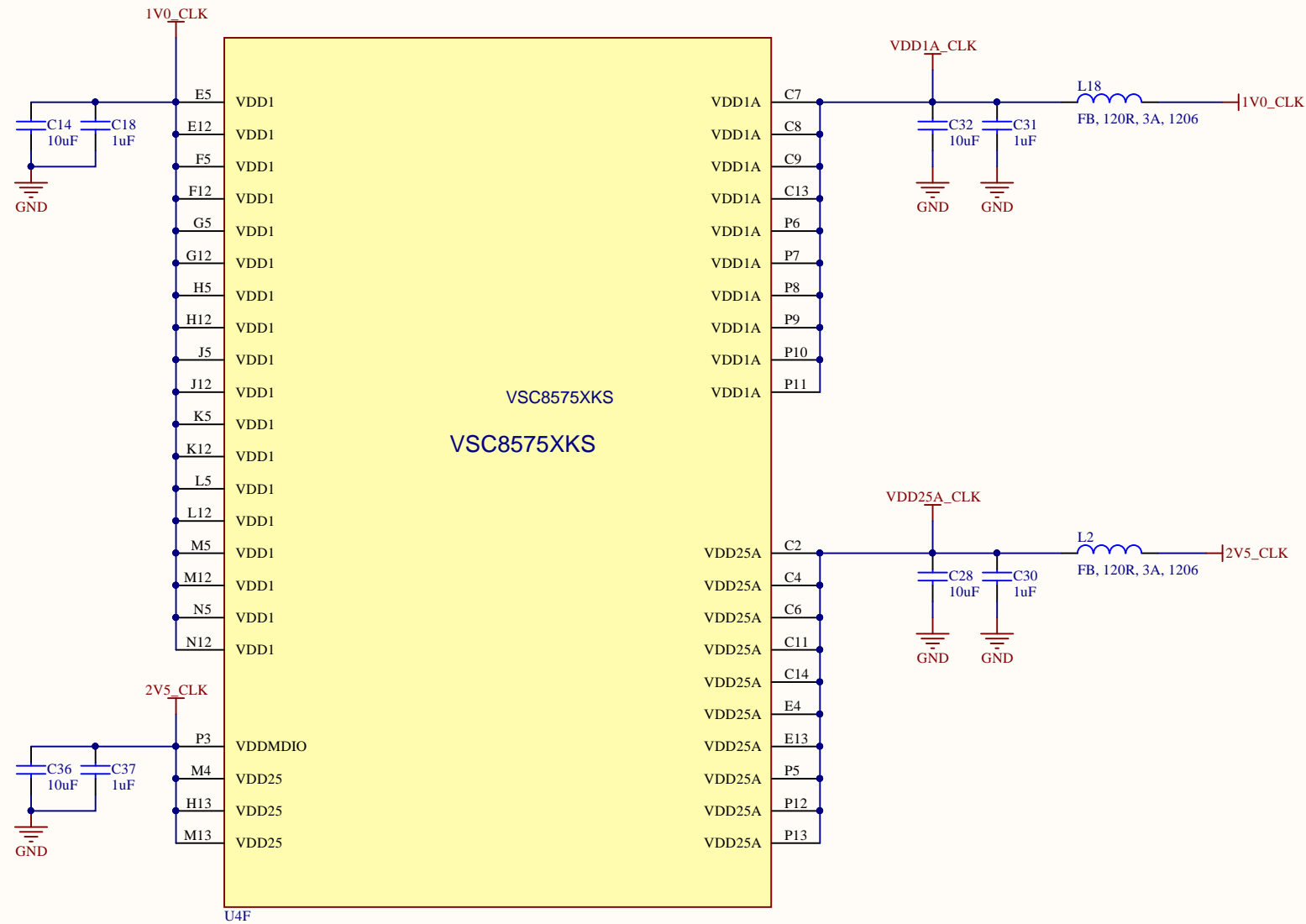
U4A

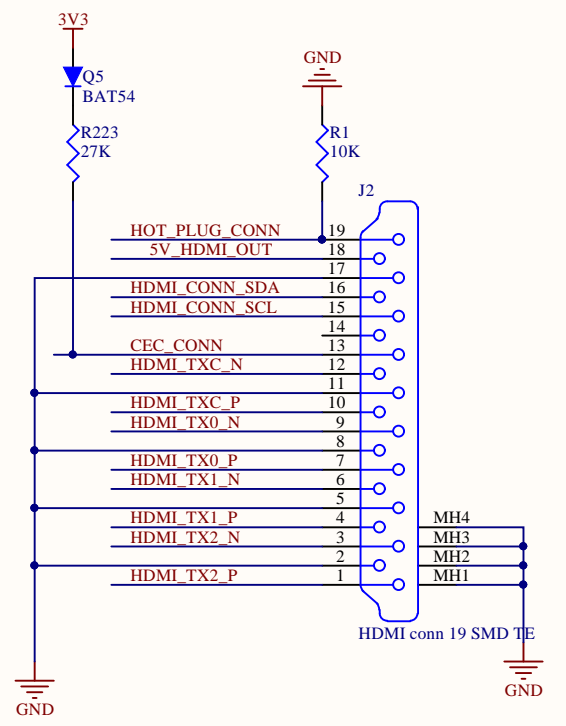
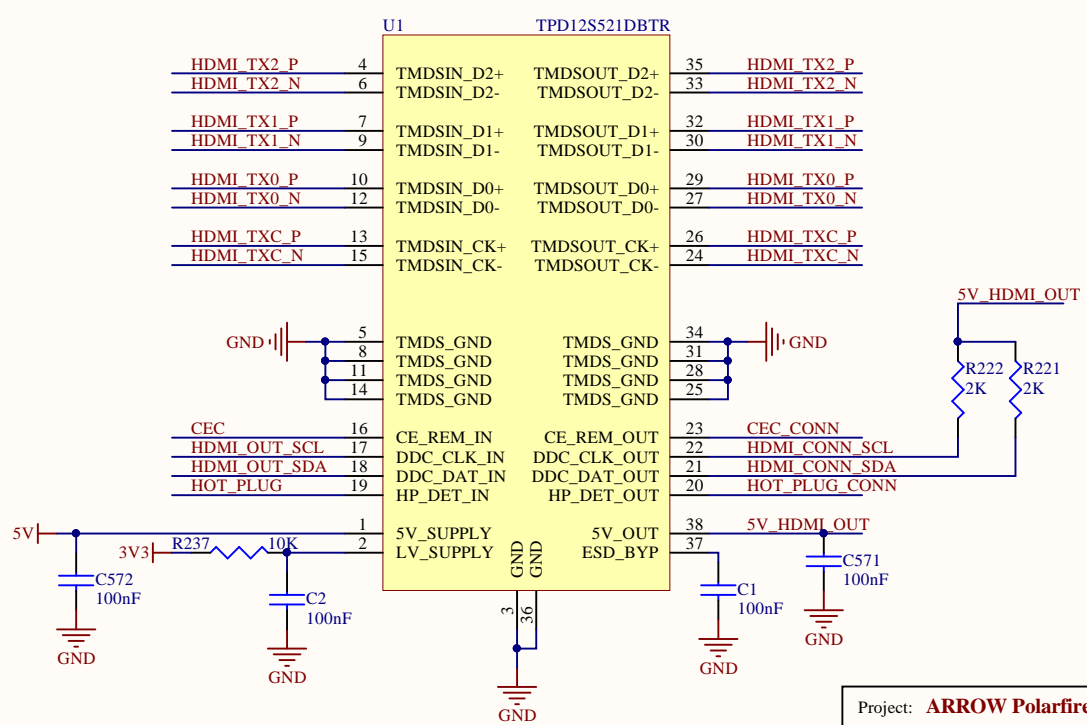
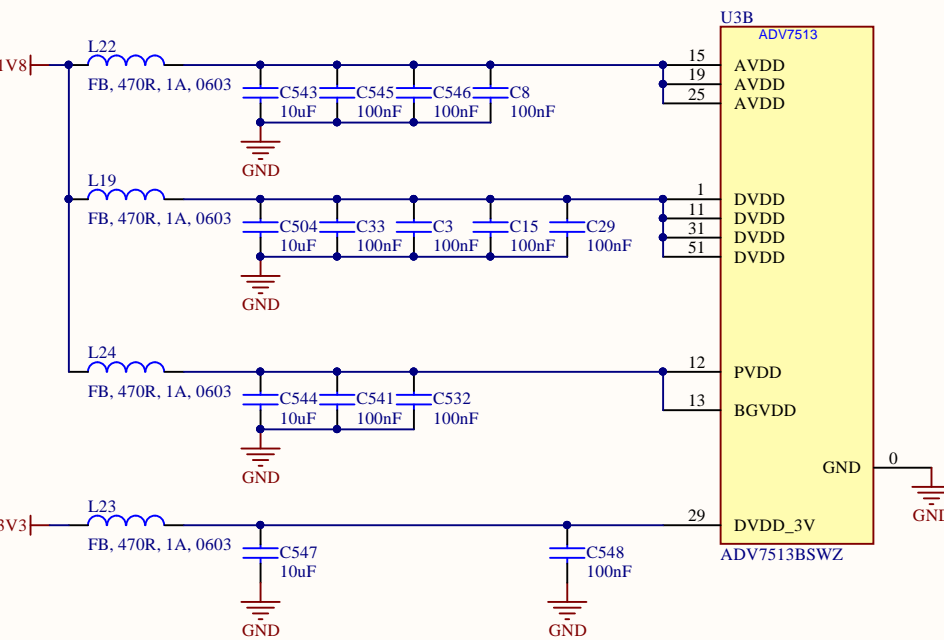
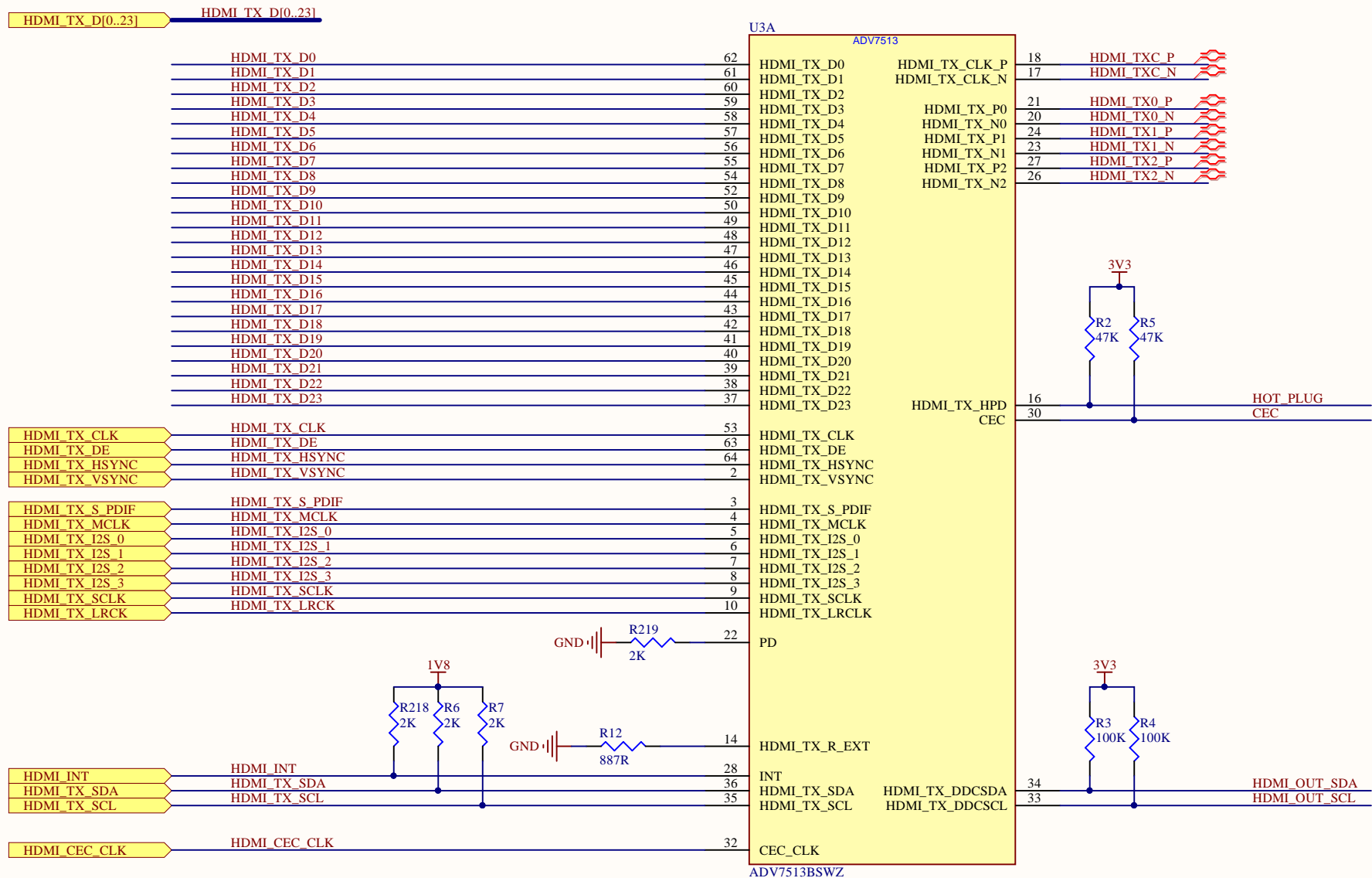


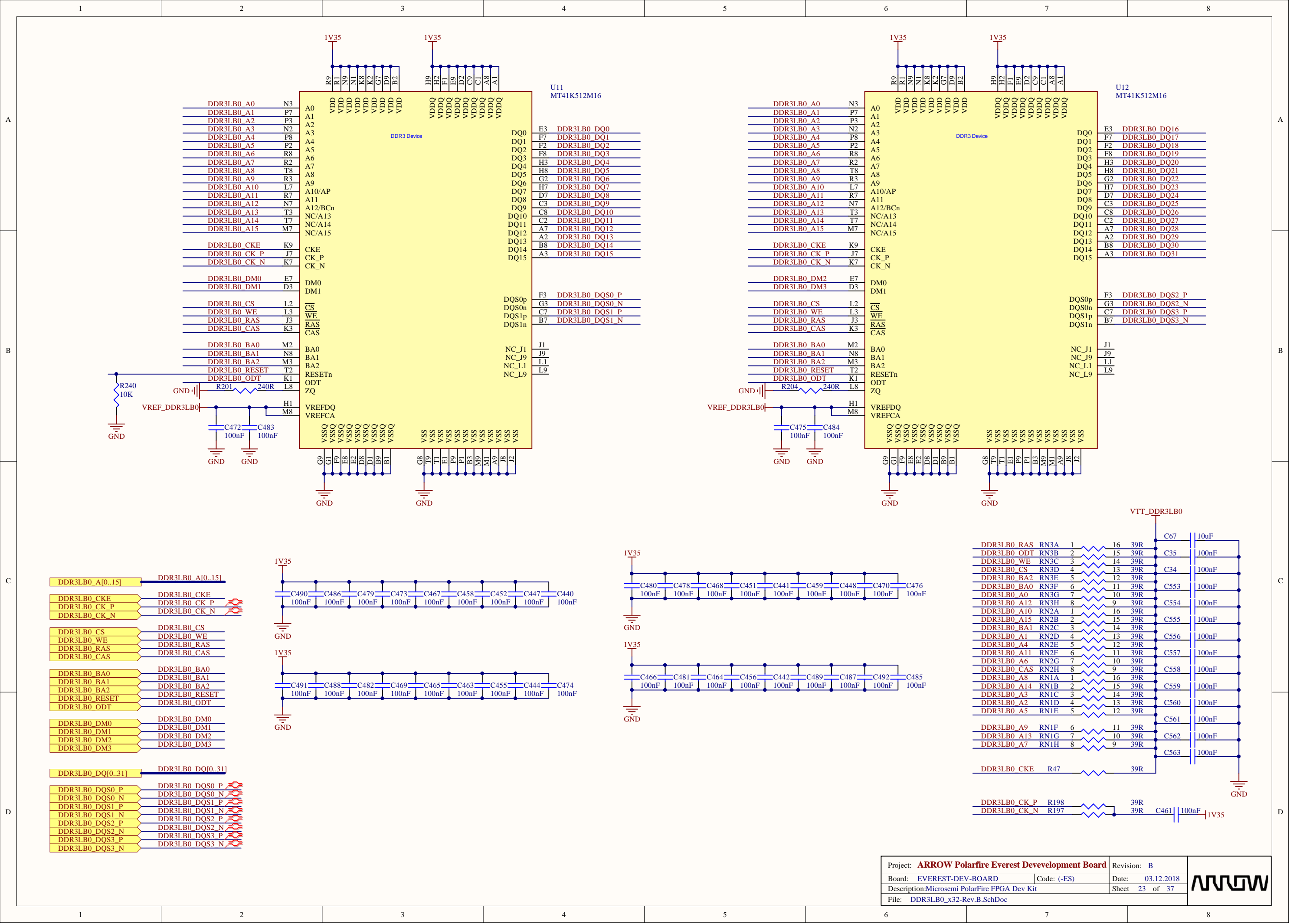
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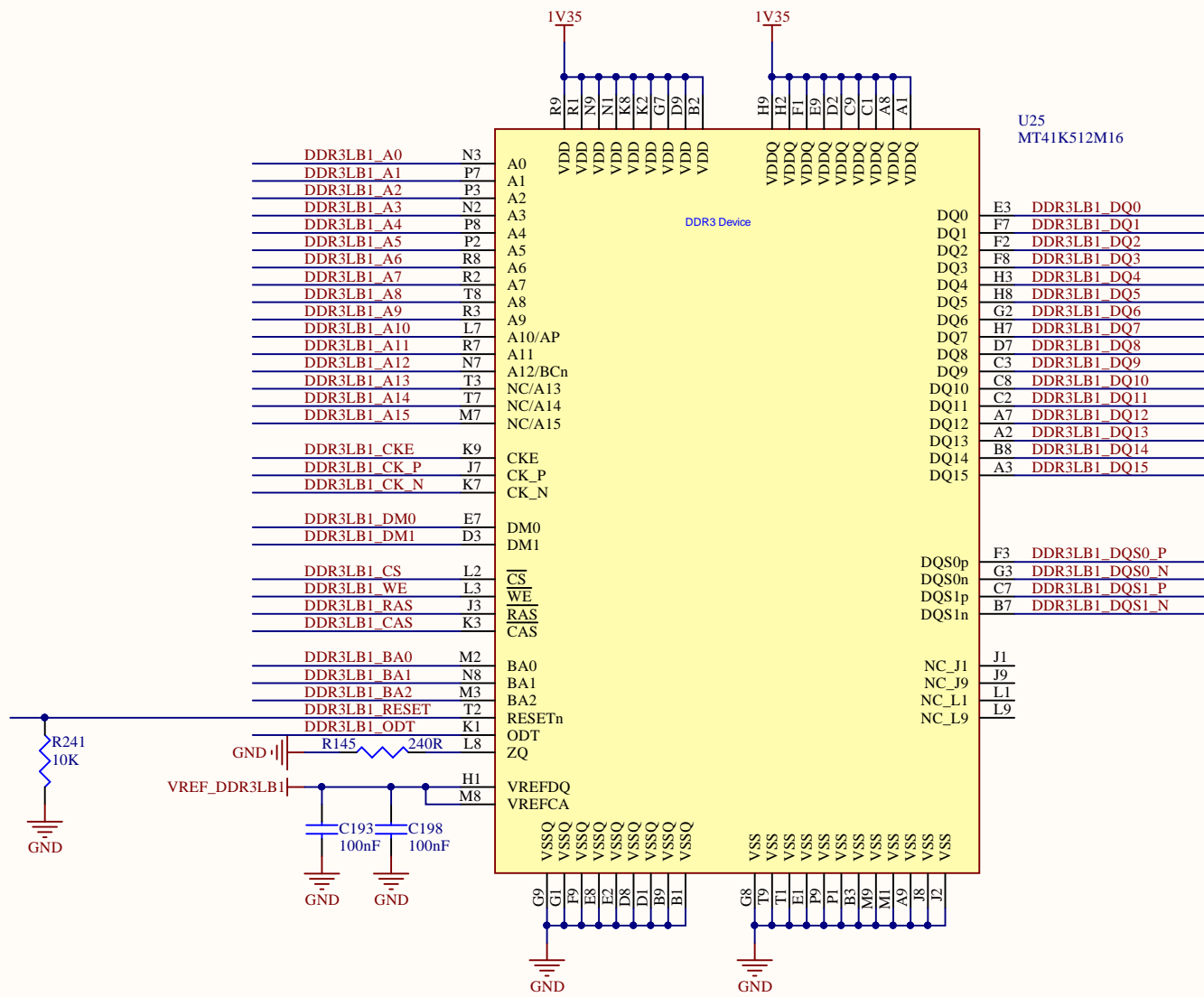










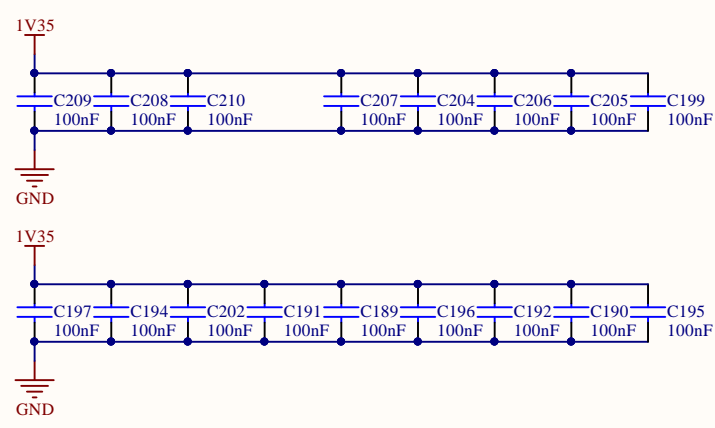
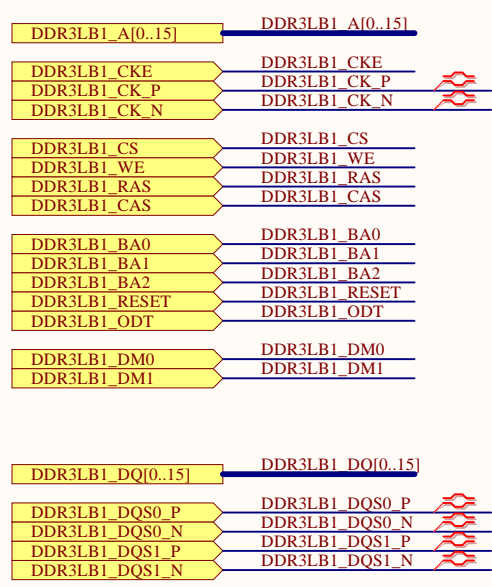
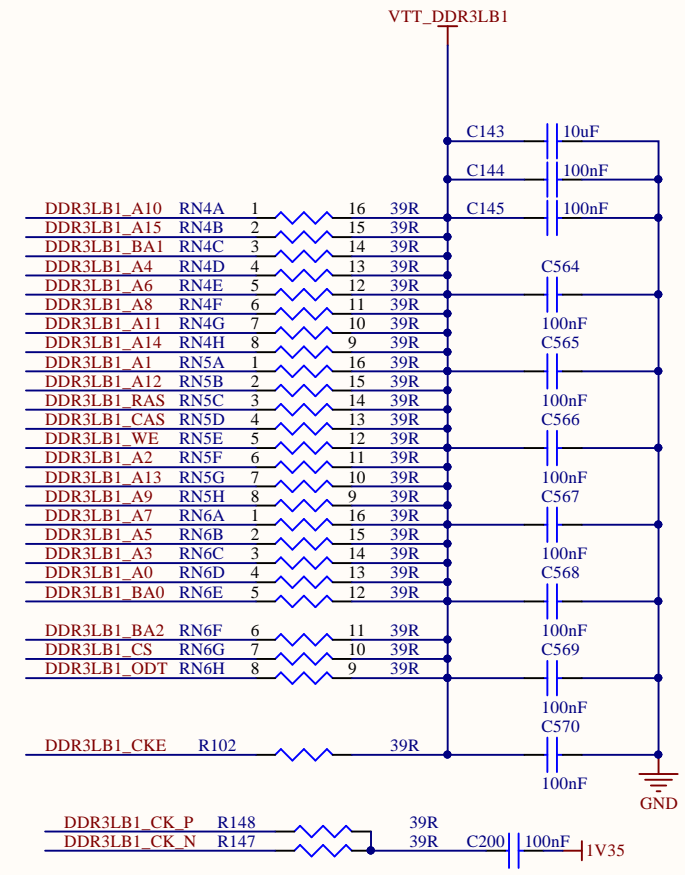


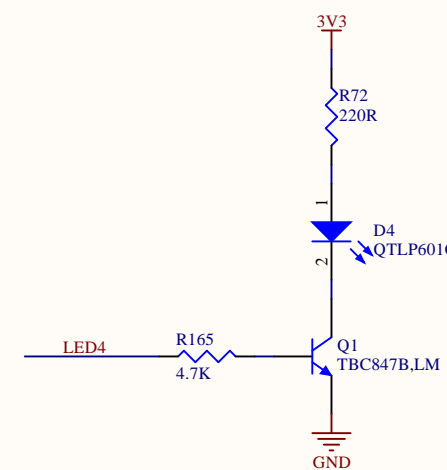
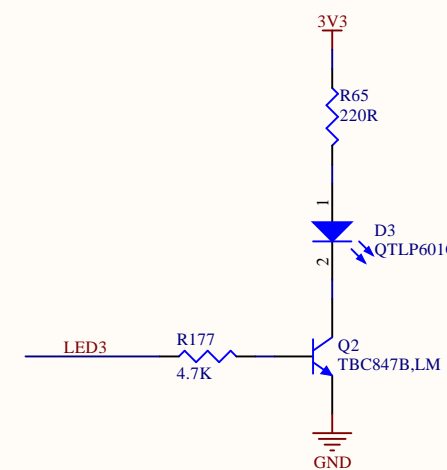
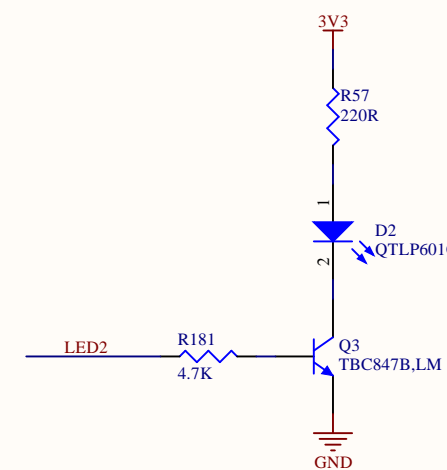
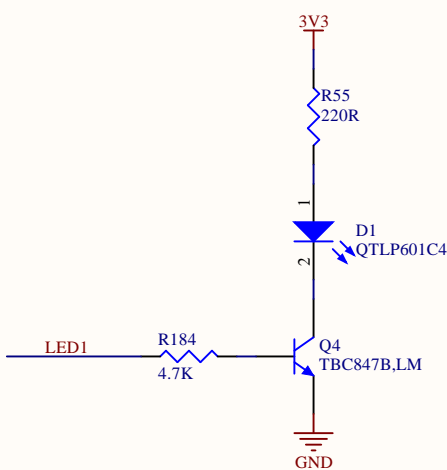
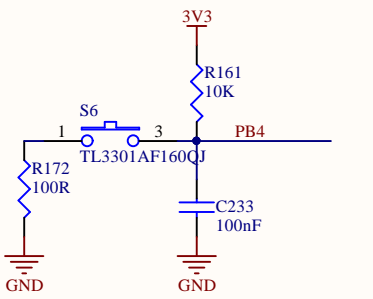
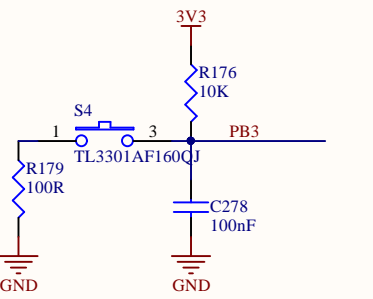
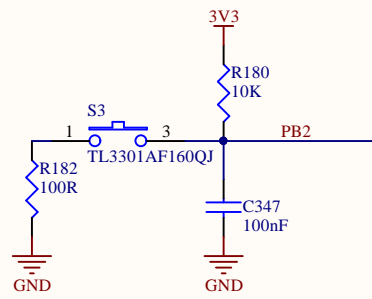
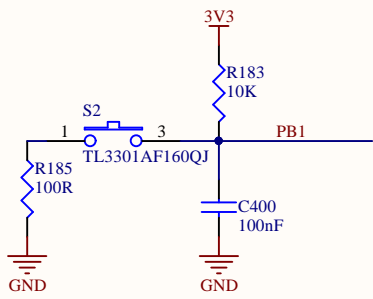
U25
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F7	DDR3LB1_DQ1
F2	DDR3LB1_DQ2
F8	DDR3LB1_DQ3
H3	DDR3LB1_DQ4
H8	DDR3LB1_DQ5
G2	DDR3LB1_DQ6
H7	DDR3LB1_DQ7
D7	DDR3LB1_DQ8
C3	DDR3LB1_DQ9
C8	DDR3LB1_DQ10
C2	DDR3LB1_DQ11
A7	DDR3LB1_DQ12
A2	DDR3LB1_DQ13
B8	DDR3LB1_DQ14
A3	DDR3LB1_DQ15

F3	DDR3LB1_DQS0_P
G3	DDR3LB1_DQS0_N
C7	DDR3LB1_DQS1_P
B7	DDR3LB1_DQS1_N

J1	NC_J1
J9	NC_J9
L1	NC_L1
L9	NC_L9





NET NAME	FPGA PIN NO	FPGA PIN NAME	BANK	Voltage Level
PB1	T4	GPIO217NB4	BANK-4	3,3V
PB2	Y8	GPIO199NB4	BANK-4	3,3V
PB3	V8	GPIO198PB4	BANK-4	3,3V
PB4	W10	GPIO200PB4	BANK-4	3,3V
LED1	U11	GPIO206NB4	BANK-4	3,3V
LED2	T5	GPIO217PB4	BANK-4	3,3V
LED3	W8	GPIO199PB4	BANK-4	3,3V
LED4	W9	GPIO201NB4	BANK-4	3,3V

