Everest PCIe End Point DDR3-Demo

Getting Started

Contents

Figures

Tables

1. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Updated version for Libero v2021.2

1.2 Revision 1.2

Updated version for Libero v12.4

1.3 Revision 1.1

Updated version for Libero v12.0

1.4 Revision 1.0

Revision 1.0 is the first publication of this document.

2. Getting Started

This demo design implements a PCIe end point and is based on the Microsemi™ PCIe end point demo guide (DG0756). Any external PCIe root-port or bridge can establish a PCIe link and access the control registers, DDR3 16 Bit, DDR3 32 Bit, and fabric memory through the BAR space. The memory read (MRd) and write (MWr) access is done by using transaction layer packets (TLPs). These TLPs are translated by the PCIe end point into AXI4 master interface transactions and accesses the fabric memory through the CoreAXI4Interconnect IP.

The device driver on the host PC allocates memory and initiates the DMA Engine in the PolarFire PCIe controller by accessing the PCIe DMA registers through BAR0. The PCIe controller has two independent DMA Engines:

• DMA Engine 0 performs DMA from host PC memory to Everest DEV Board memory.
• DMA Engine 1 performs DMA from Everest DEV Board memory to host PC memory.

The PCIe demo application[1] uses the device driver to initiates the CoreAXI4DMA controller IP core to perform DMA between DDR3 memory and LSRAM. The two used channels of the CoreAXI4DMA controller perform the following actions:

Table 1: CoreAXI4DMA channels actions

DMA channel	DMA	
	from	to
0	DDR3 16 Bit DDR3 32 Bit	DDR3 32 Bit, LSRAM LSRAM
1	DDR3 32 Bit LSRAM	DDR3 16 Bit DDR3 16 Bit, DDR3 32 Bit

Beside that the PCIe demo application can initiate the CoreAXI4DMA controller through the USB UART interface on the Everest DEV Board to perform onboard transfers from and to the different memory locations, if no PCIe slot is available.
For further information please refer to the above mentioned Microsemi™ design guide DG0756.

[1] http://soc.microsemi.com/download/rsc/?f=mpf_dg0756_liberosocpolarfirev2p2_df

2.1 Prerequisites

For the Everest PCIe End Point DDR3-Demo the following is needed:

Item	**Quantity**
Everest DEV Board	1
12 V / 5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for UART / Programming interface to PC	1
Free one-year Libero Silver software license	1
host PC with PCIe x4 slot	1

Note: The Everest DEV Board offers an on-board FlashPro5 programmer, which can be used to program and debug with Identify, SmartDebug and embedded application software using SoftConsole.

2.2 Handling the Board

Pay attention to the following points while handling or operating the board:

Handle the board with electrostatic discharge (ESD) precautions to avoid damage.

For information about ESD precautions see

https://www.microsemi.com/documentportal/doc_view/126483-esd-appnote.

2.3 Board-Setup

2.3.1 Toggle-Switch S1 – PCIe

SWITCH	PCIe LANES
S1-1 (marking)	x4
S1-2	x1

2.3.2 Toggle -Switch S5 – SC SPI-Flash enable

SWITCH	SC SPI-FLASH
S5-1 (marking)	DISABLE
S5-2	ENABLE

2.3.3 DIP-Switch S8 – FMC Voltage Selector

SWITCH	FMC VOLTAGE
S8-1 off, S8-2 off	1.8 V
S8-1 on, S8-2 off	2.5 V
S8-1 off, S8-2 on	undefined (not recommended)
S8-1 on, S8-2 on	3.3 V

2.3.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

SWITCH	VDDAUX2 & VDDAUX5
S9-1 (marking)	2.5 V
S9-2	FMC voltage

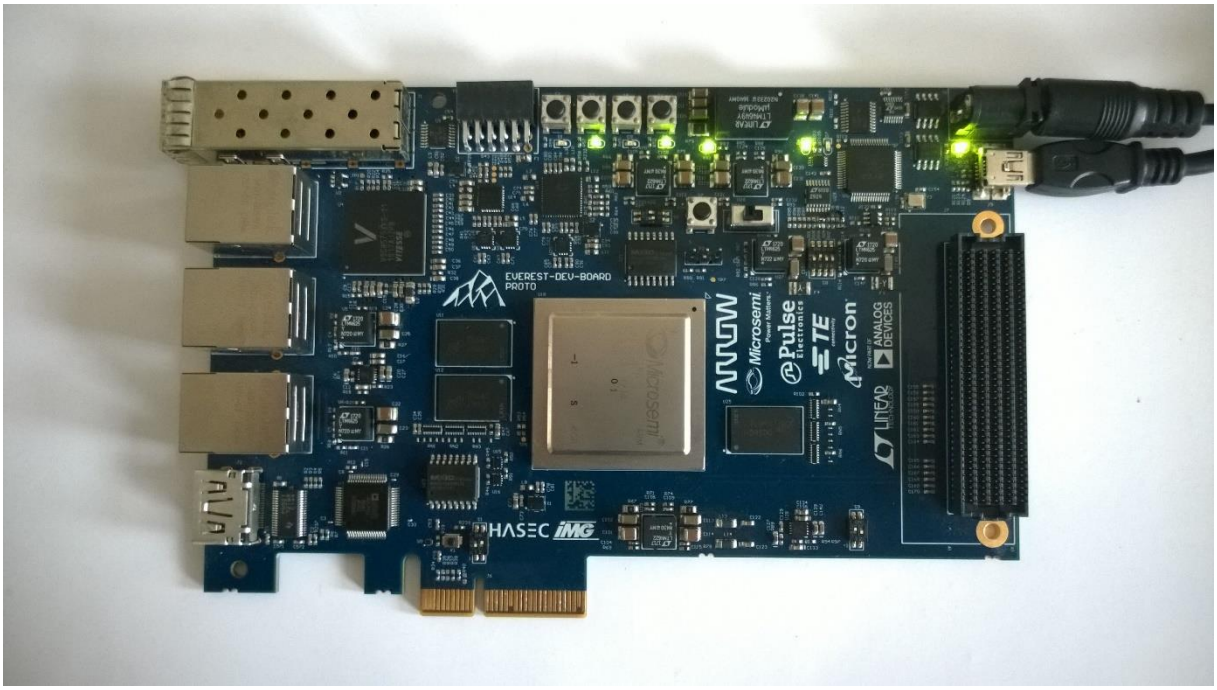


Figure 1: Everest Board

2.4 Powering up the Board

The Everest DEV Board is powered up using either the 12 V DC jack or the PCIe connector. For programming connect it although with your computer using USB mini B connector J9.

3. Demo Design

3.1 Prerequisites

Table 2: Software / IP Requirements

Software	**Version**
Libero SoC	V2021.2
Synplify Pro	R-2021.03M
FlashPro Express	V2021.2
IP	
COREAHBTOAPB3	v3.2.101
COREAXI4INTERCONNECT	v2.8.103
COREAXITOAHBL	v3.6.101
PF_CCC	V2.2.100
PF_CLK_DIV	v1.0.103
COREAXI4DMACONTROLLER	v2.0.100
CoreAHBLite	v5.5.101
CoreAPB3	v4.2.100
COREUART	v5.7.100
PF_NGMUX	v1.0.101
PF_OSC	v1.0.102
PF_INIT_MONITOR	v2.0.204
PF_TX_PLL	v2.0.300
PF_DDR3	v2.4.112
CORERESET_PF	v2.3.100
PF_SRAM_AHBL_AXI	v1.2.108
PF_TPSRAM	v1.1.108
PF_PCIE	v2.0.104
PF_XCVR_REF_CLK	v1.0.103

Before you start you have to make sure, that all cores are downloaded to your local vault.

3.2 Design Implementation

The following table lists the clock frequencies used in the design.

Table 3: Hardware Design Clock Frequencies

clock source	used by	frequency (MHz)
REF_CLK_0	CCC_111_MHz	50
CCC_111MHz *OUT0_FABCLK_0*	PF_DDR3_SS_0 *PLL_REF_CLK*, PF_DDR3_32Bit_0 *PLL_REF_CLK*,	111.111
CCC_111MHz *OUT1_FABCLK_0*	PF_RESET_0 *CLK*, AXI4_Interconnect_0 *ACLK*, SRAM_AXI_0 *ACLK*, CoreDMA_IO_CTRL_0 *CLOCK*, PCIe_EP_0 *AXI_CLK*	200
PF_DDR3_16Bit_0 *SYS_CLK*,	AXI4_Interconnect_0 *S_CLK2*	166.6665
PF_DDR3_32Bit_0 *SYS_CLK*,	AXI4_Interconnect_0 *S_CLK4*	166.6665

3.2.1 Top Level

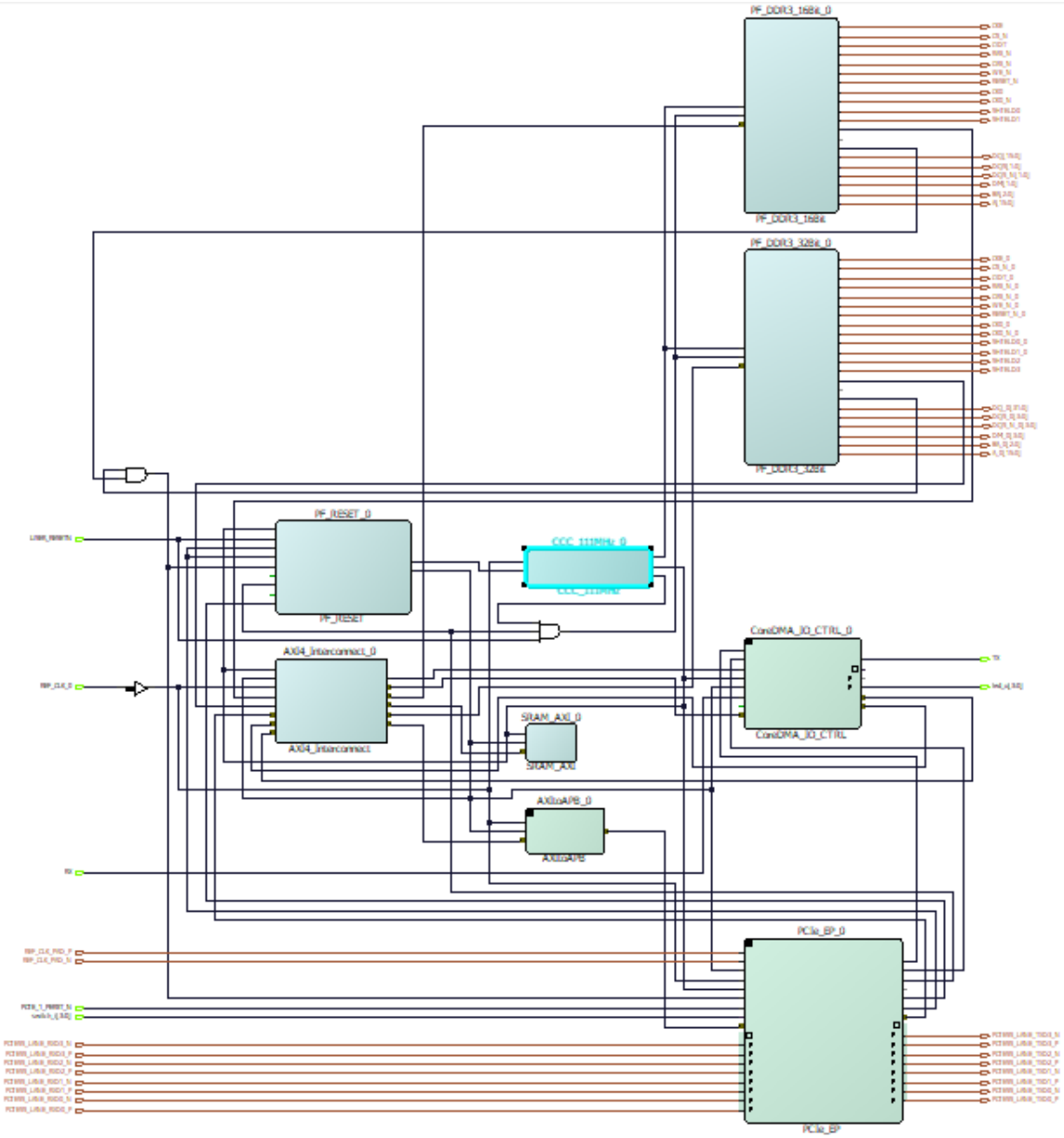


Figure 2: Design Implementation – PCIe_EP_Demo (top level)

3.2.2 Smart Design PCIe_EP

Figure 3 shows the design implementation of the PCIe_EP smart design.

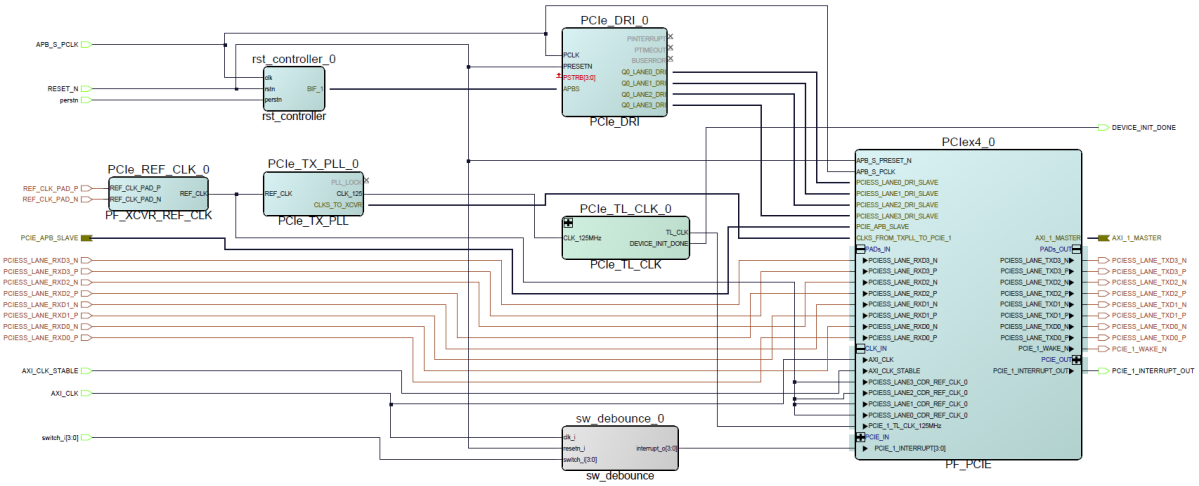


Figure 3: Design Implementation – PCIe_EP

The design is already fully implemented and ready to be programmed on the Everest Board. The board has to be connected with the power supply and to the PC with the USB cable. All drivers have to be installed (which should happen automatically when plugged in the first time) To program the design, there are two possibilities:

- Programming via Libero PolarFire SoC: Programming is started with the “Run PROGRAM Action” Button in the Design Flow Pane
- Programming via FlashPro Software: There is a STAPL-File (“Bitstream\PCIe_EP_Demo.stp”) which can be programmed with the FlashPro Software. A new FlashPro project has to be generated and the programming file loaded into.

3.3 Configuration

3.3.1 PCIe end point – ip-core PF_PCIE

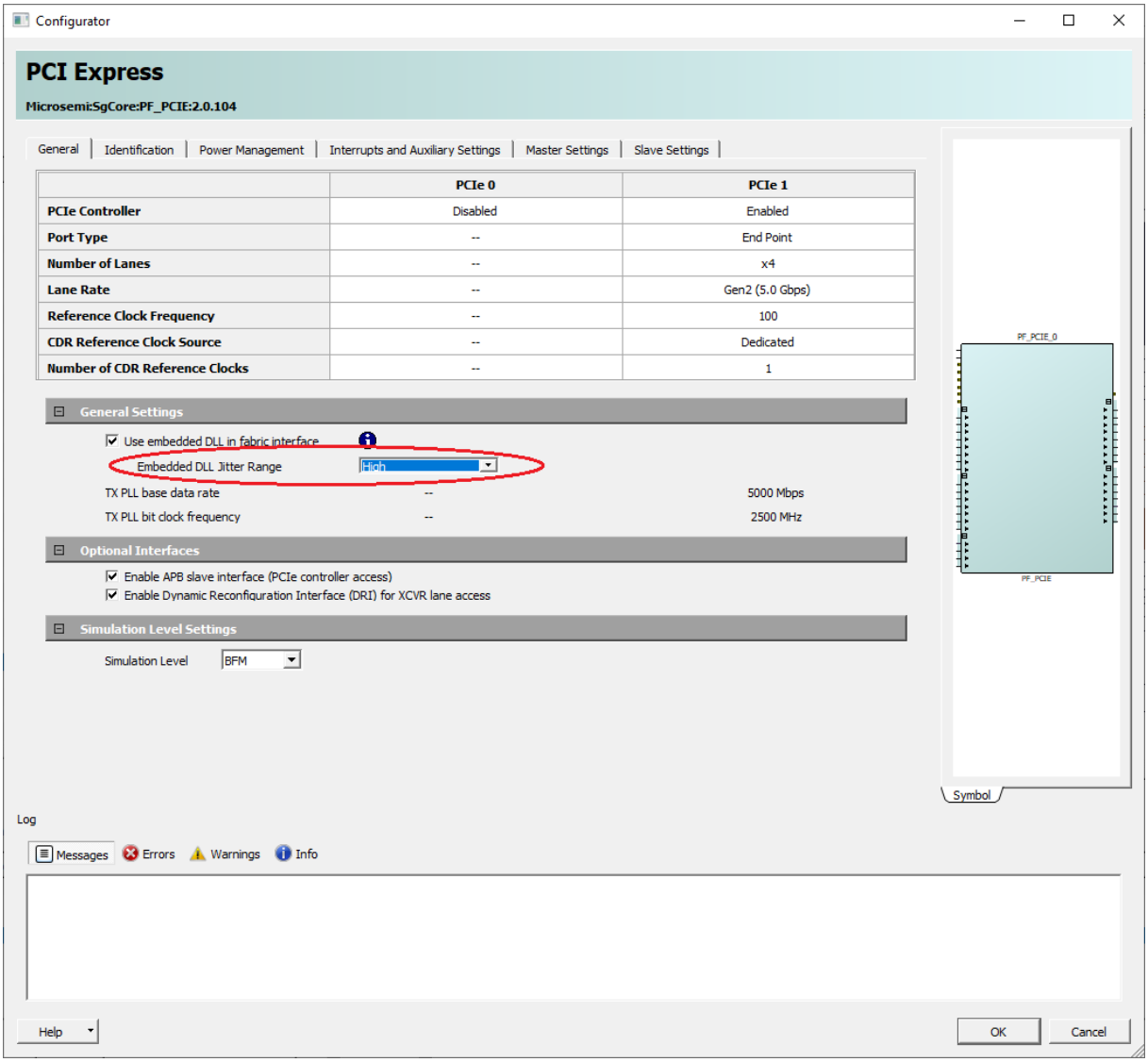


Figure 4: Configuration PF_PCIE - General tab

Please make sure, that embedded DLL jitter range is set to high.

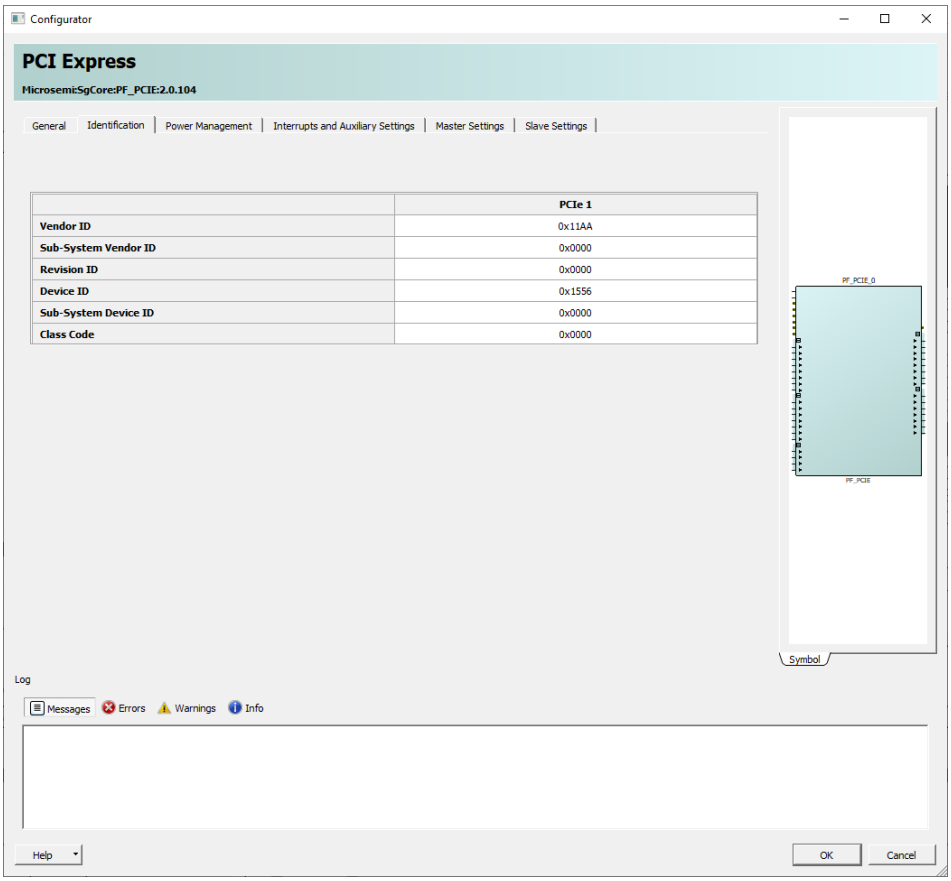


Figure 5: Configuration PF_PCIE - Identification tab

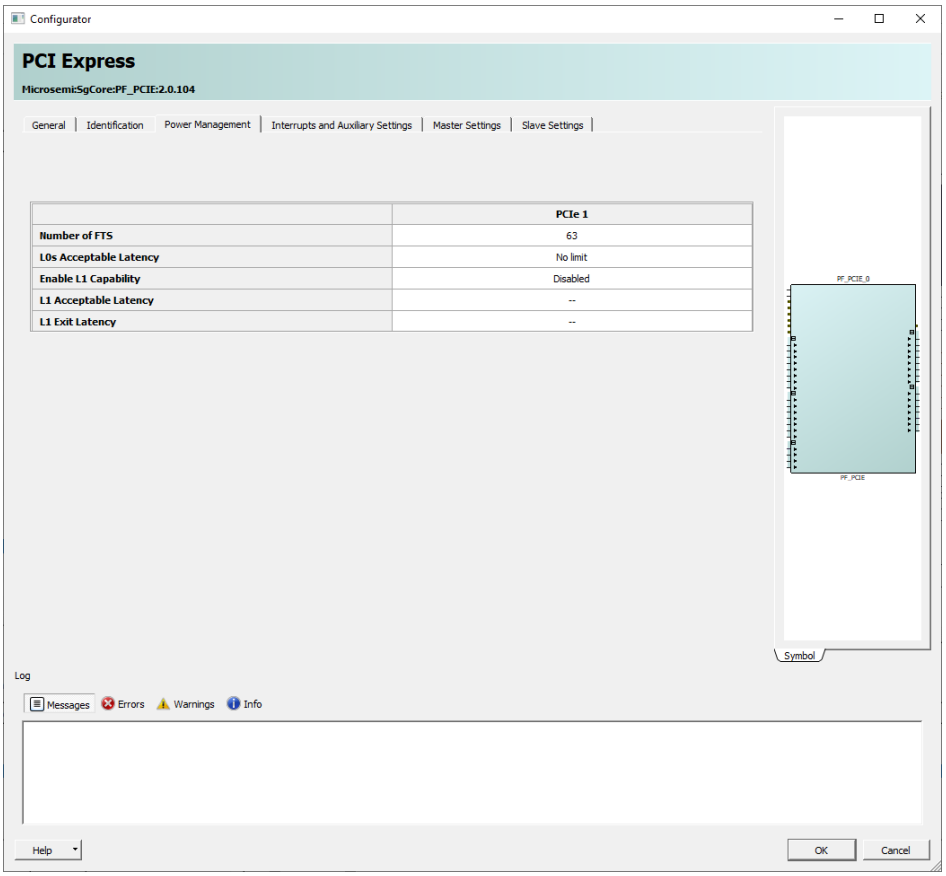


Figure 6: Configuration PF_PCIE - Power Management tab

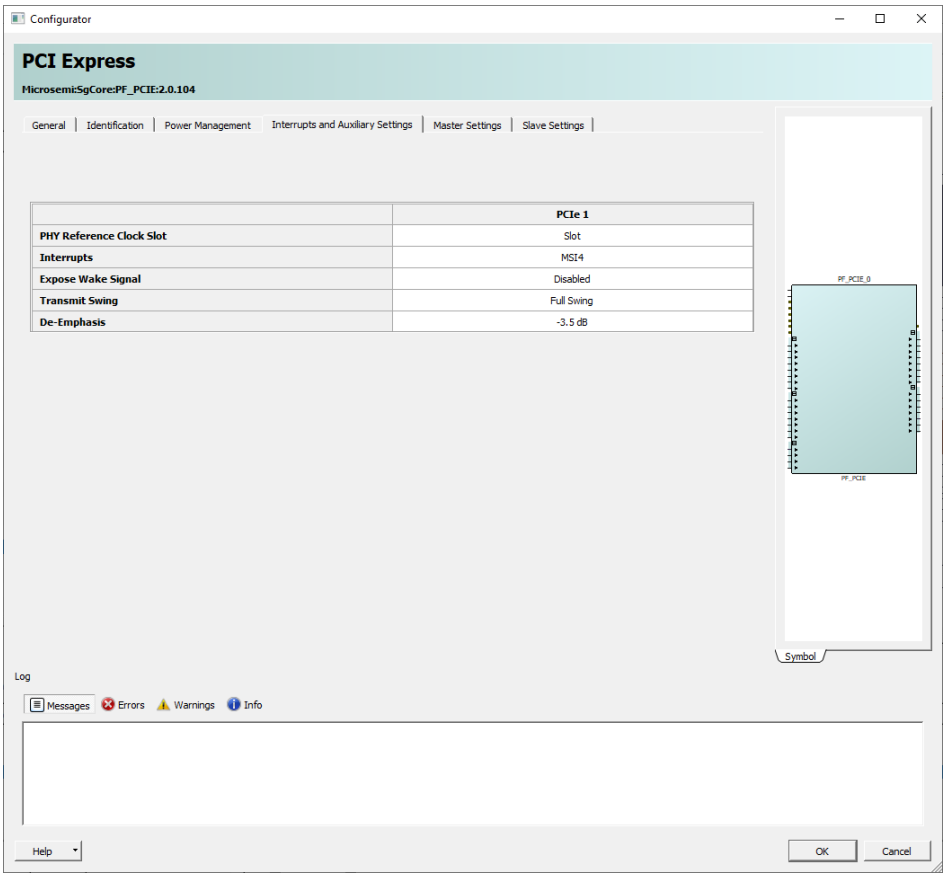


Figure 7: Configuration PF_PCIE - Interrupts and Auxiliary Settings tab

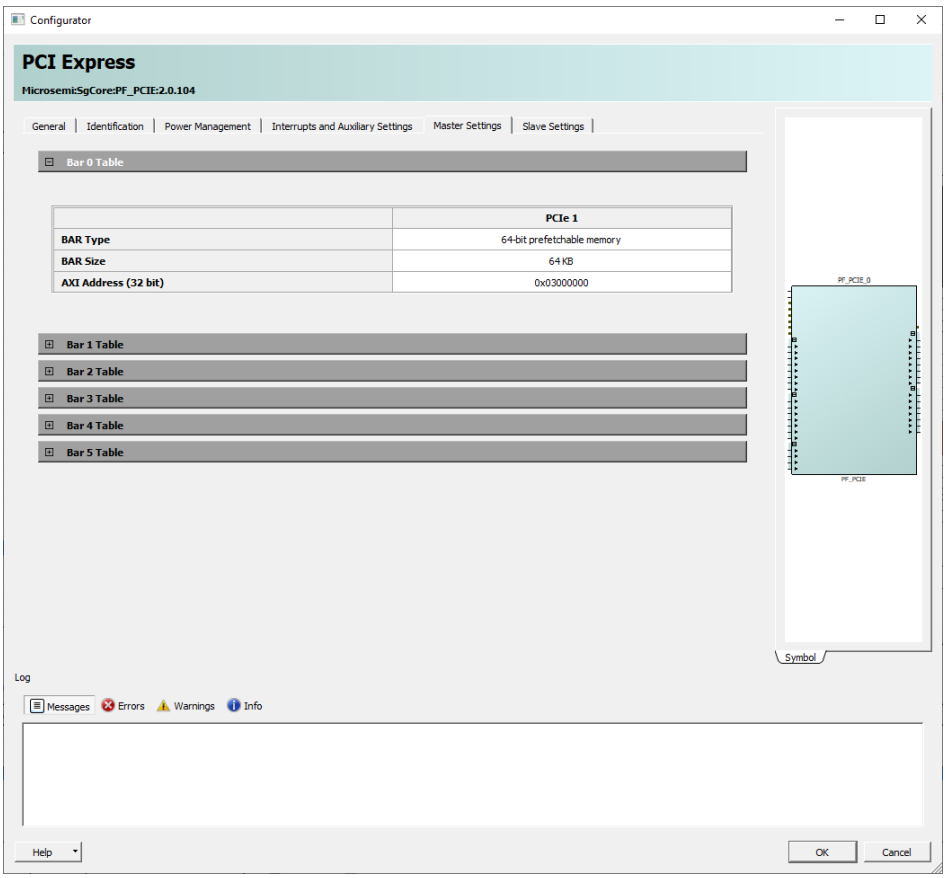


Figure 8: Configuration PF_PCIE - Master Settings tab BAR 0

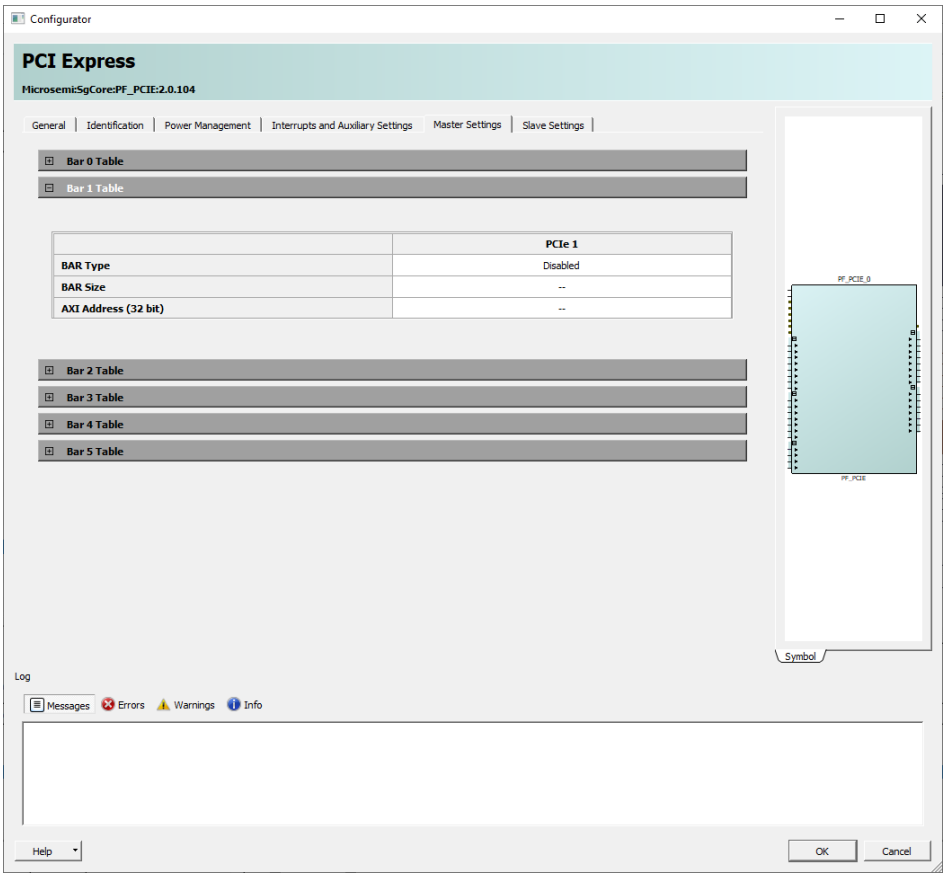


Figure 9: Configuration PF_PCIE - Master Settings tab BAR 1 (same for BAR 3 to 5)

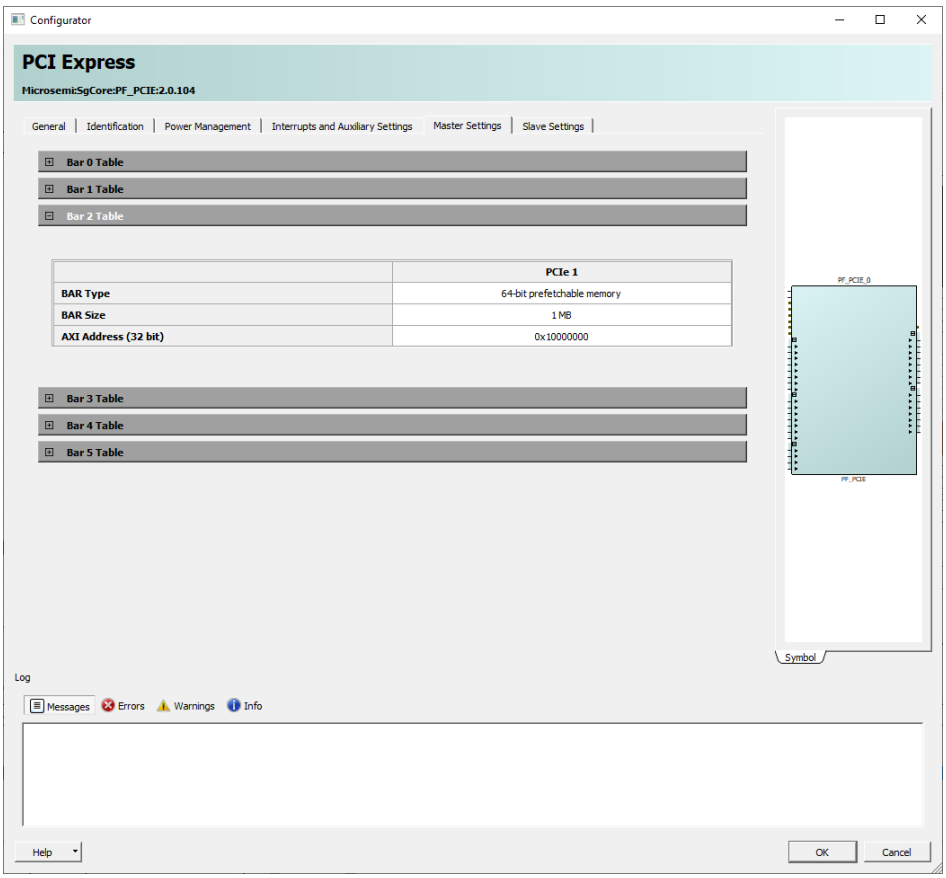


Figure 10: Configuration PF_PCIE - Master Settings tab BAR 2

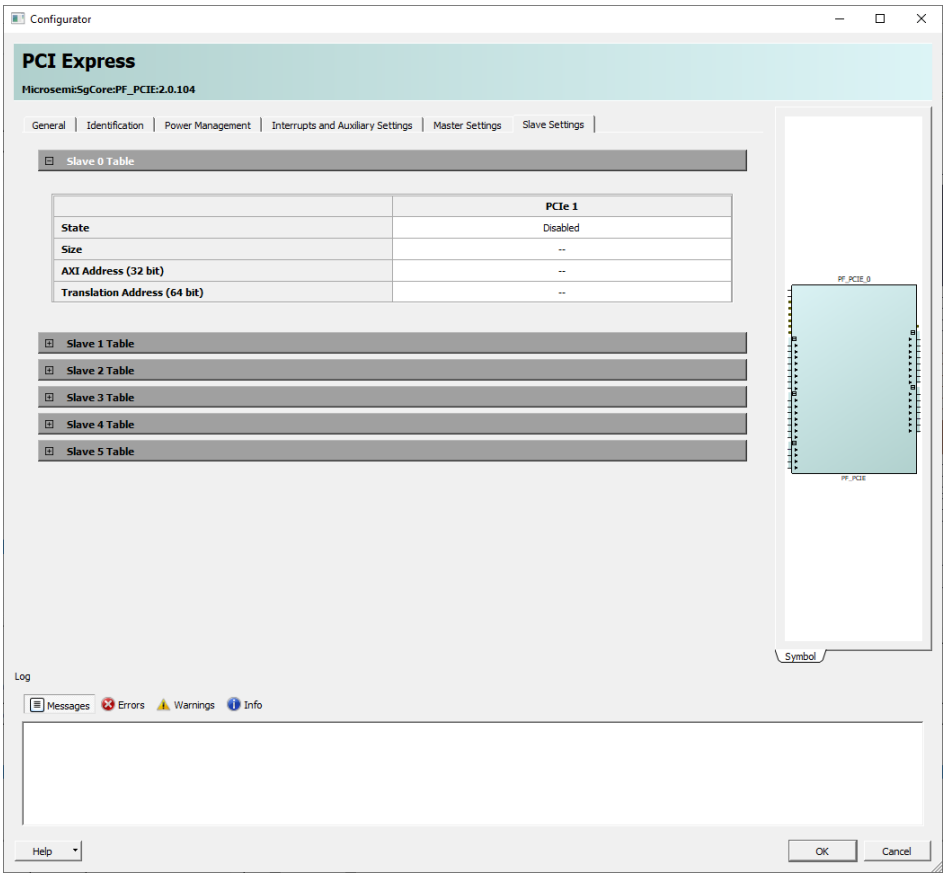
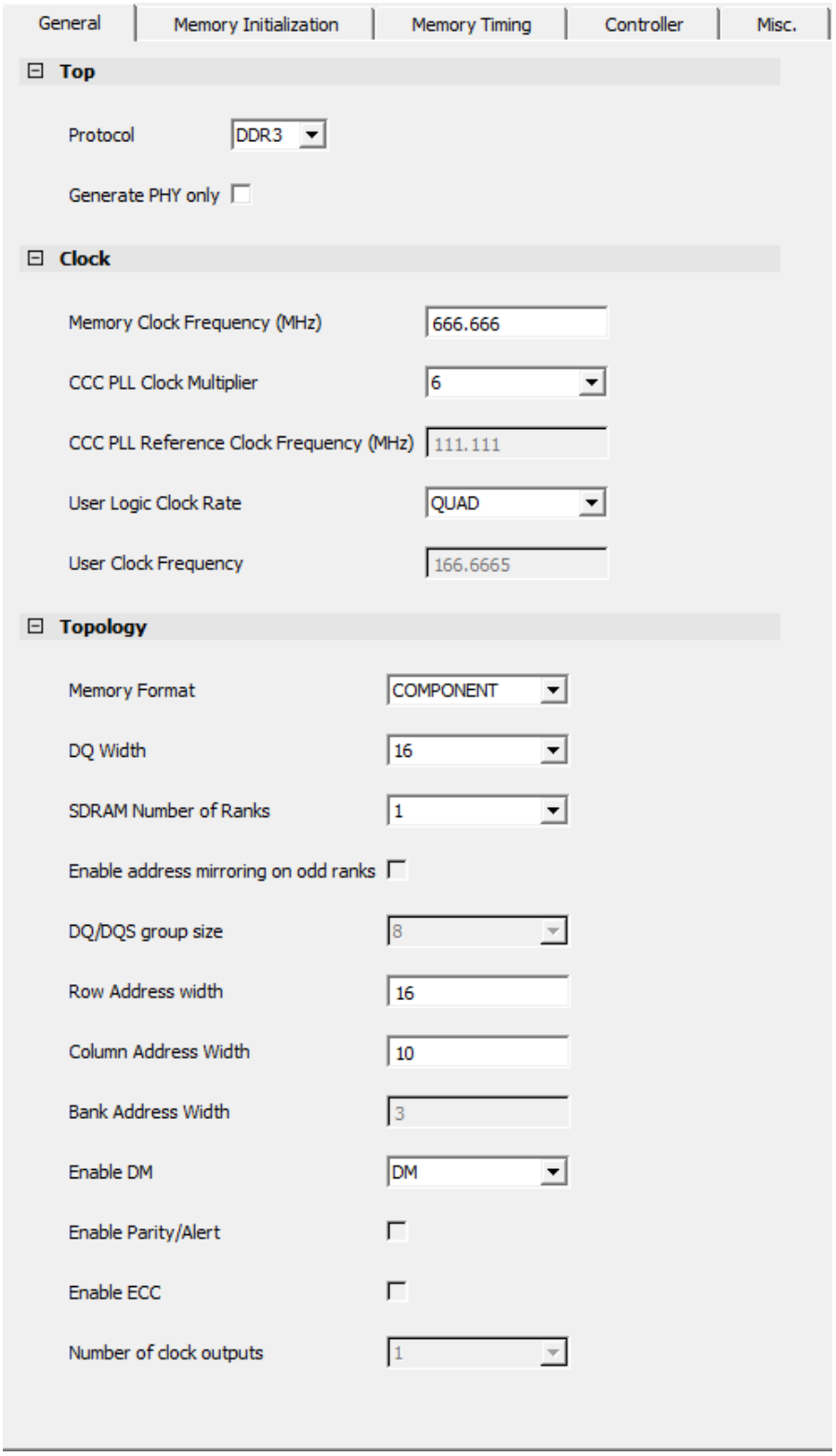


Figure 11: Configuration PF_PCIE - Slave Settings tab BAR 0 (same for BAR 1 to 5)

3.3.2 DDR3 controller – ip-core PF_DDR3

The configuration for both DDR3 controllers differs only in DQ width (16 for DDR3 16 Bit and 32 for DDR 32 Bit) and instance number (0 for DDR3 16 Bit and 1 for DDR 32 Bit). All other settings are the same.



Set DQ to 32 for 32 Bit DDR3

Figure 12: Configuration PF_DDR3 - General tab

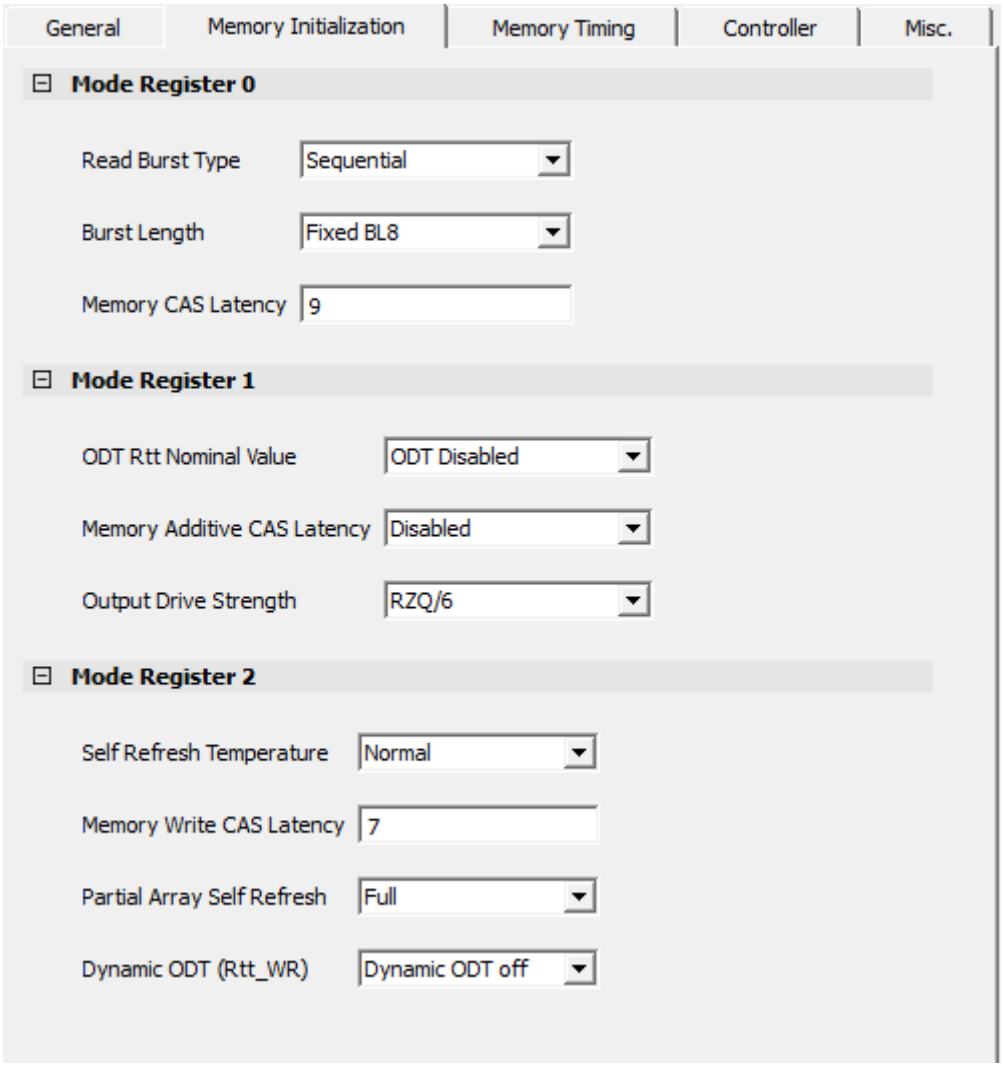


Figure 13: Configuration PF_DDR3 - Memory Initialization tab

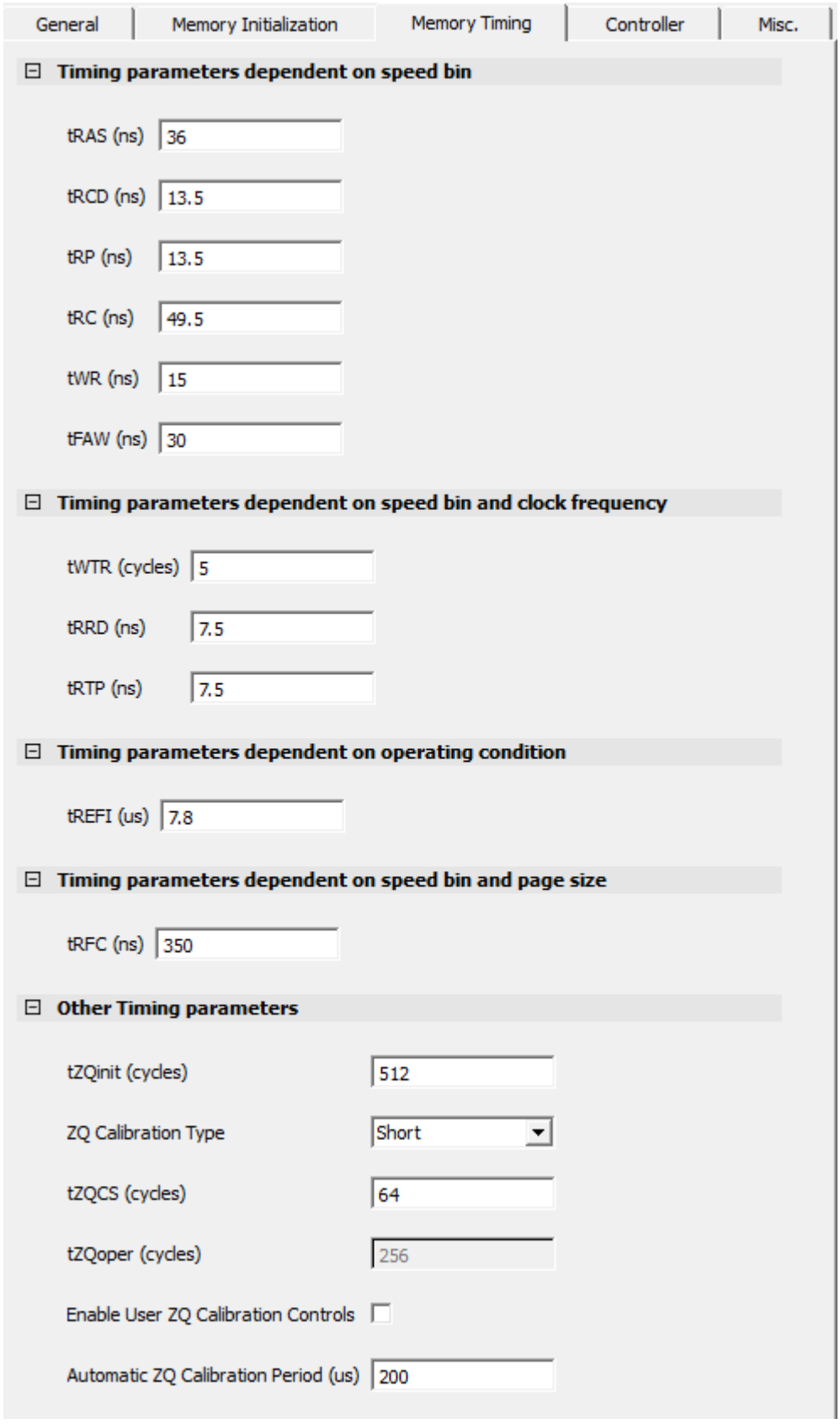
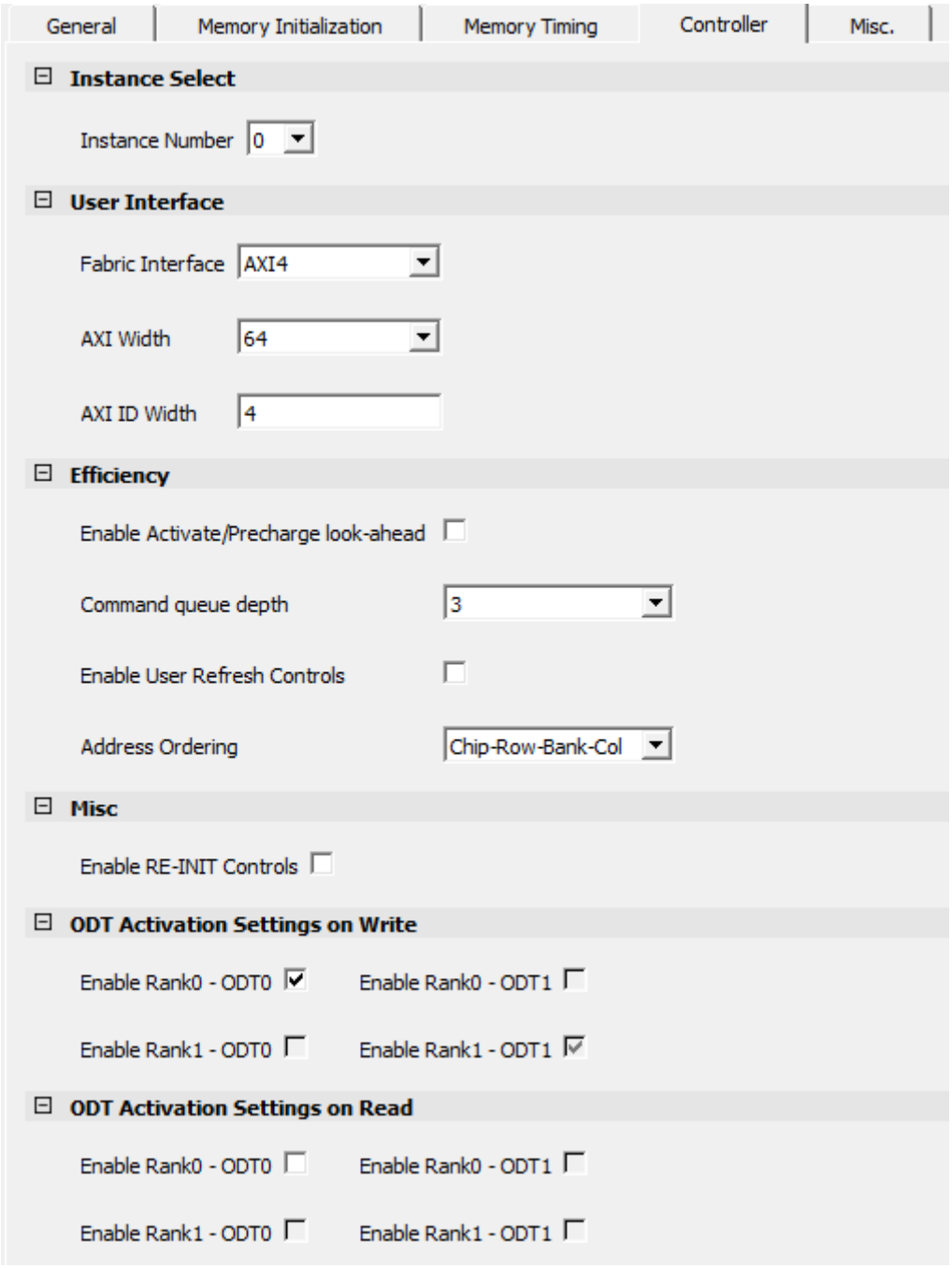


Figure 14: Configuration PF_DDR3 - Memory Timing tab



Set Instance Number to 1 for 32 Bit DDR3

Figure 15: Configuration PF_DDR3 - Controller tab

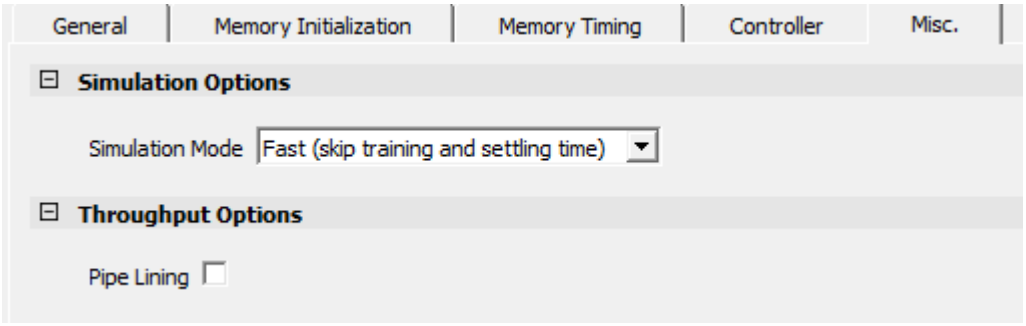


Figure 16: Configuration PF_DDR3 - Misc. tab

3.3.3 AXI4 Interconnect – COREAXI4INTERCONNECT

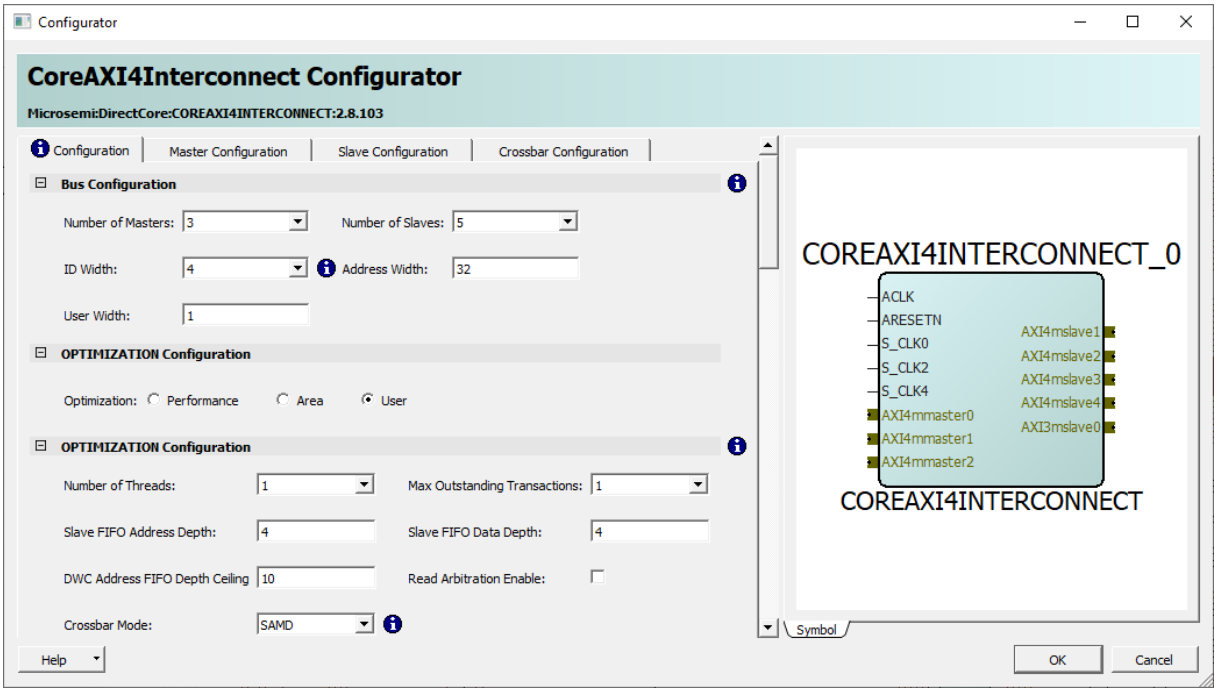


Figure 17: Configuration COREAXI4INTERCONNECT - Configuration tab

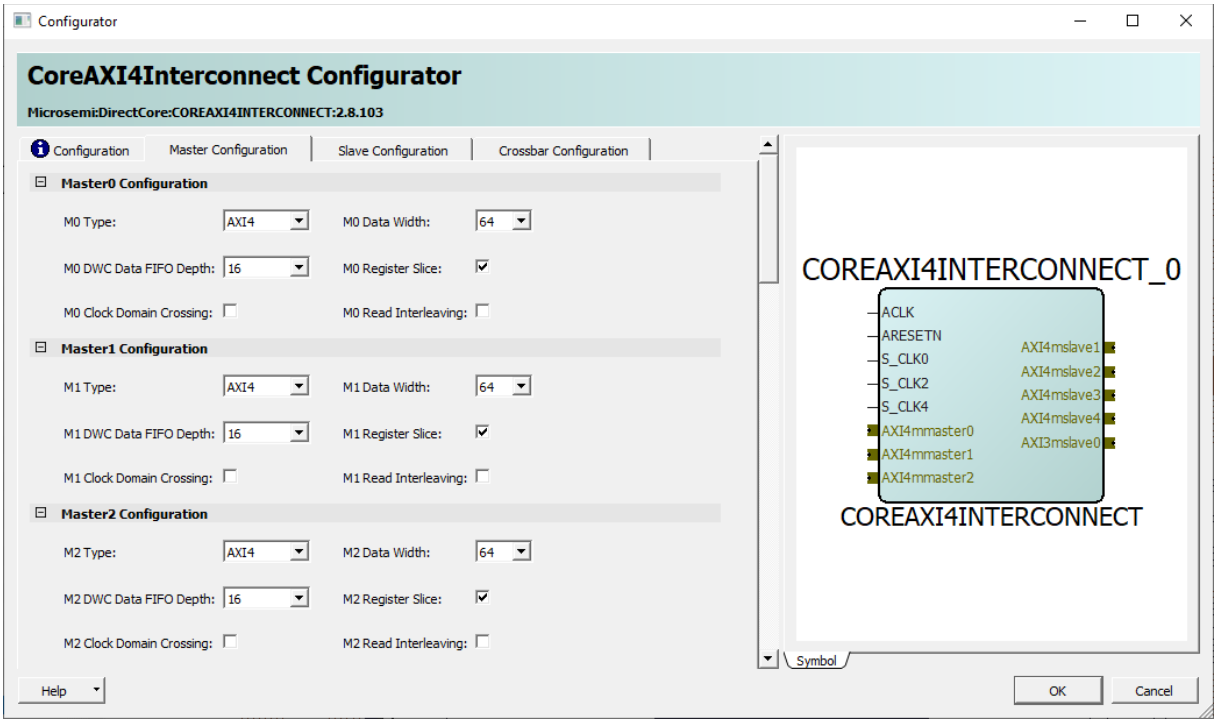


Figure 18: Configuration COREAXI4INTERCONNECT - Master Configuration tab

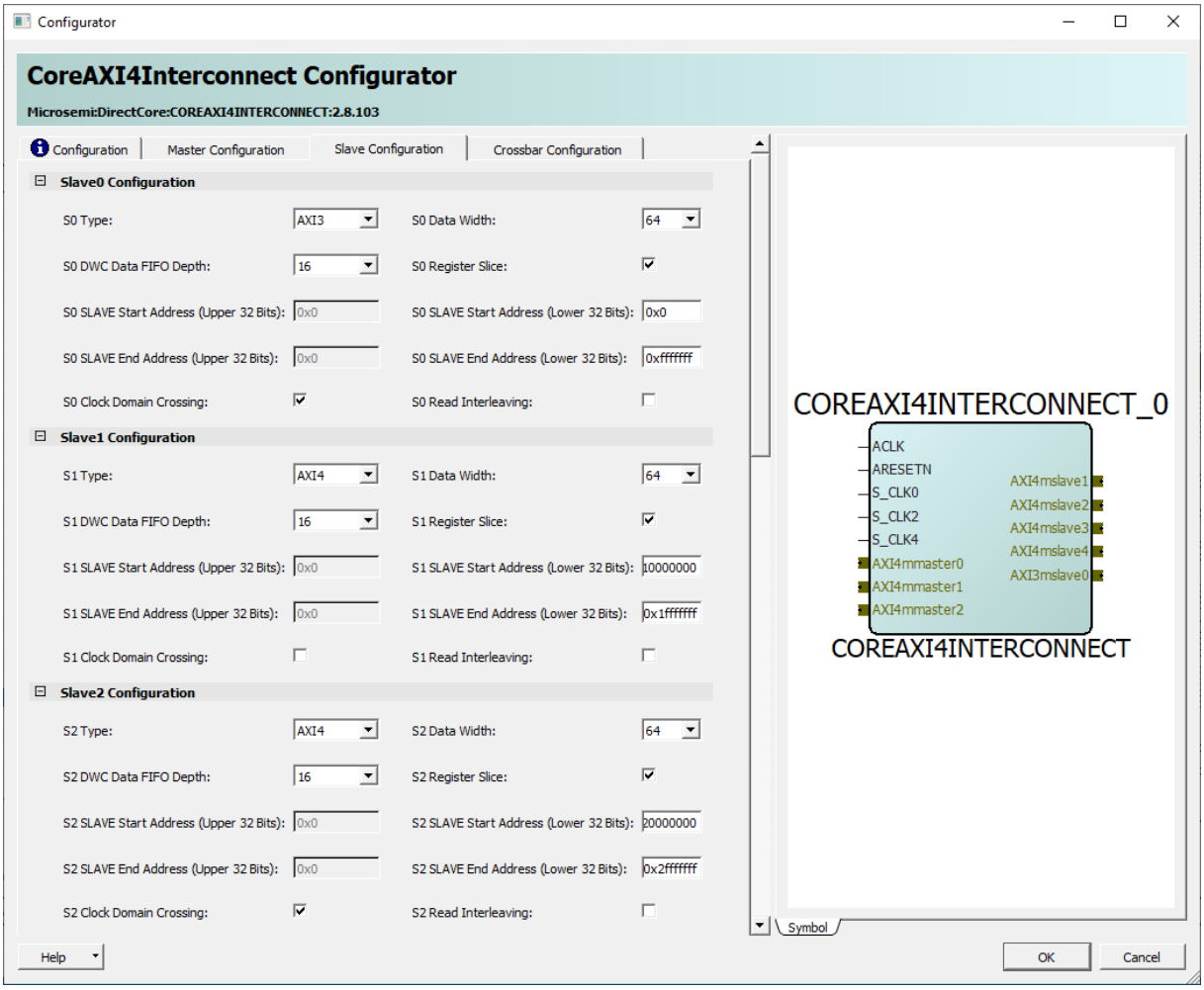


Figure 19: Configuration COREAXI4INTERCONNECT - Slave Configuration tab, Slave 0 to 2

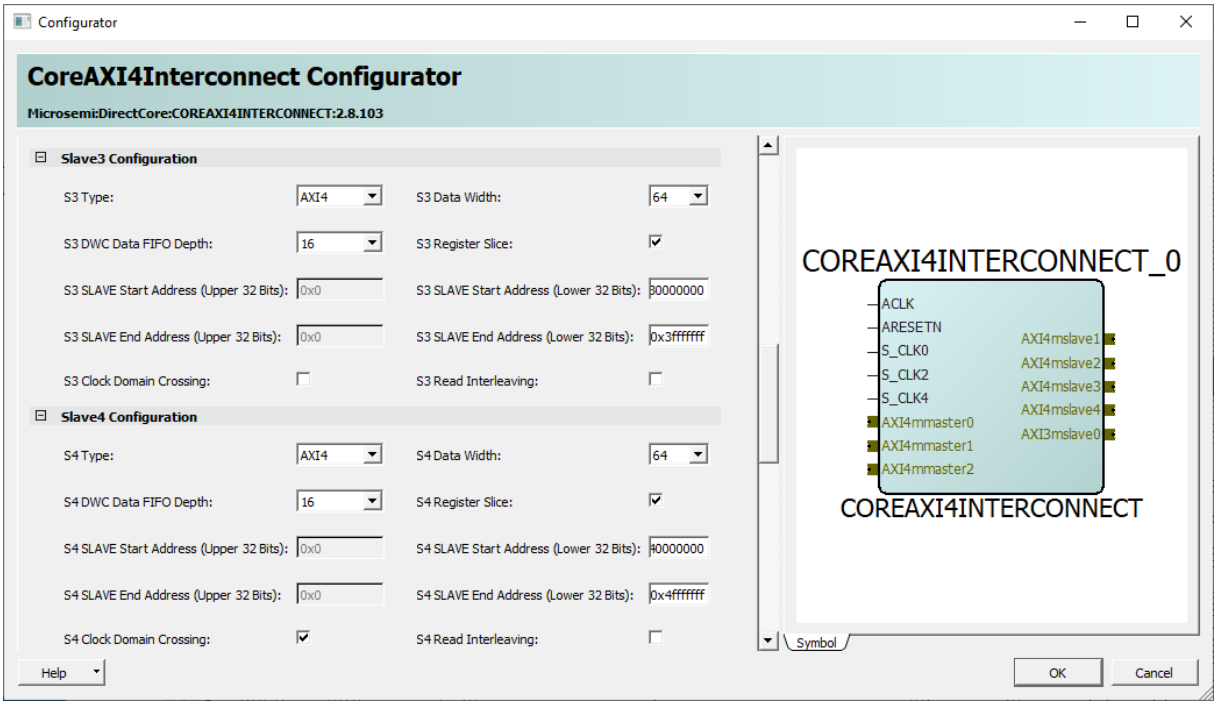


Figure 20: Configuration COREAXI4INTERCONNECT - Slave Configuration tab, Slave 3 and 4

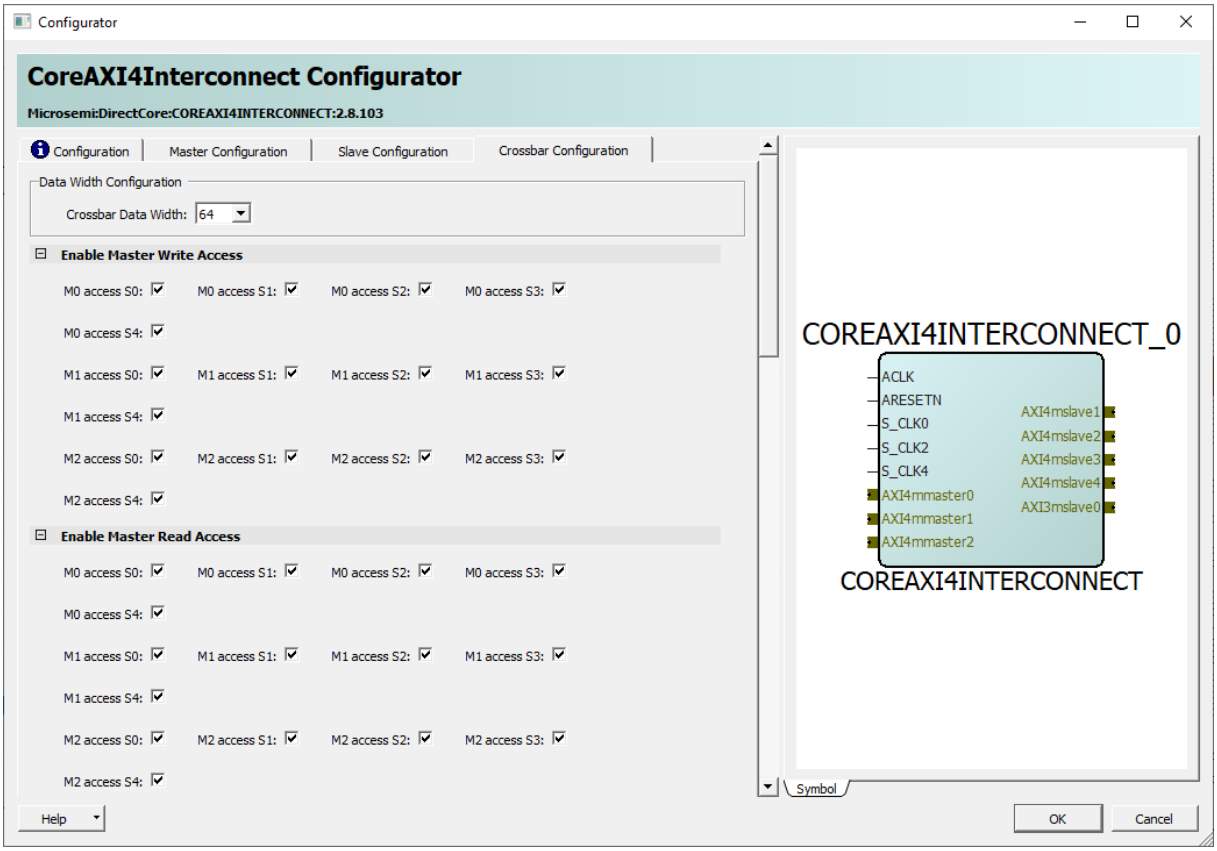


Figure 21: Configuration COREAXI4INTERCONNECT - Crossbar Configuration tab (all checkboxes are checked)

4. Running the Demo

This section describes how to install and use the Microsemi™ PCIe Demo application. The PolarFire PCIe demo application is a simple graphic user interface (GUI) that runs on the host PC to communicate with the PolarFire PCIe end point device. It provides PCIe link status, driver information, and demo controls. The PolarFire PCIe demo application invokes the PCIe driver installed on the host PC and provides commands to the driver according to the selection made. This section also describes how to connect the kit to the Host PC PCIe Slot. If the host PC does not offer a PCIe slot, the DMA between DDR3 16 Bit, DDR3 32 Bit and LSRAM can be exercised through the USB UART interface on the Everest DEV Board.

4.1 Installing the Microemi™ PCIe Demo Application

To install the demo application:

1. Install the GUI_Installer (setup.exe) from the following design files folder: mpf_dg0756_liberosocpolarfirev2p1_df\GUI_Installer.
2. Double-click the setup.exe in the provided GUI installation (GUI_Installer\setup.exe).
3. Apply default options as shown in the following figure.

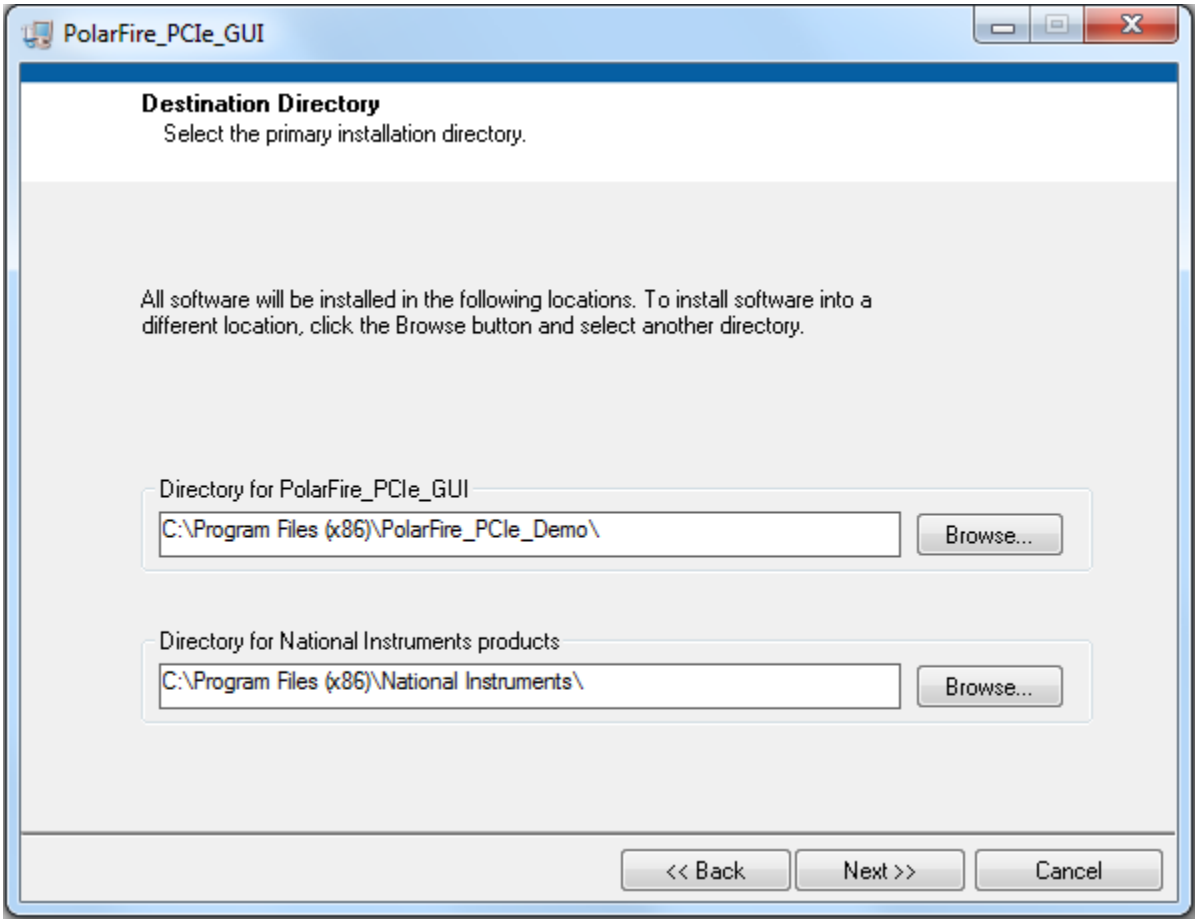


Figure 22: Installing the Microsemi PCIe Demo Application

4. Click **Next** to start the installation.

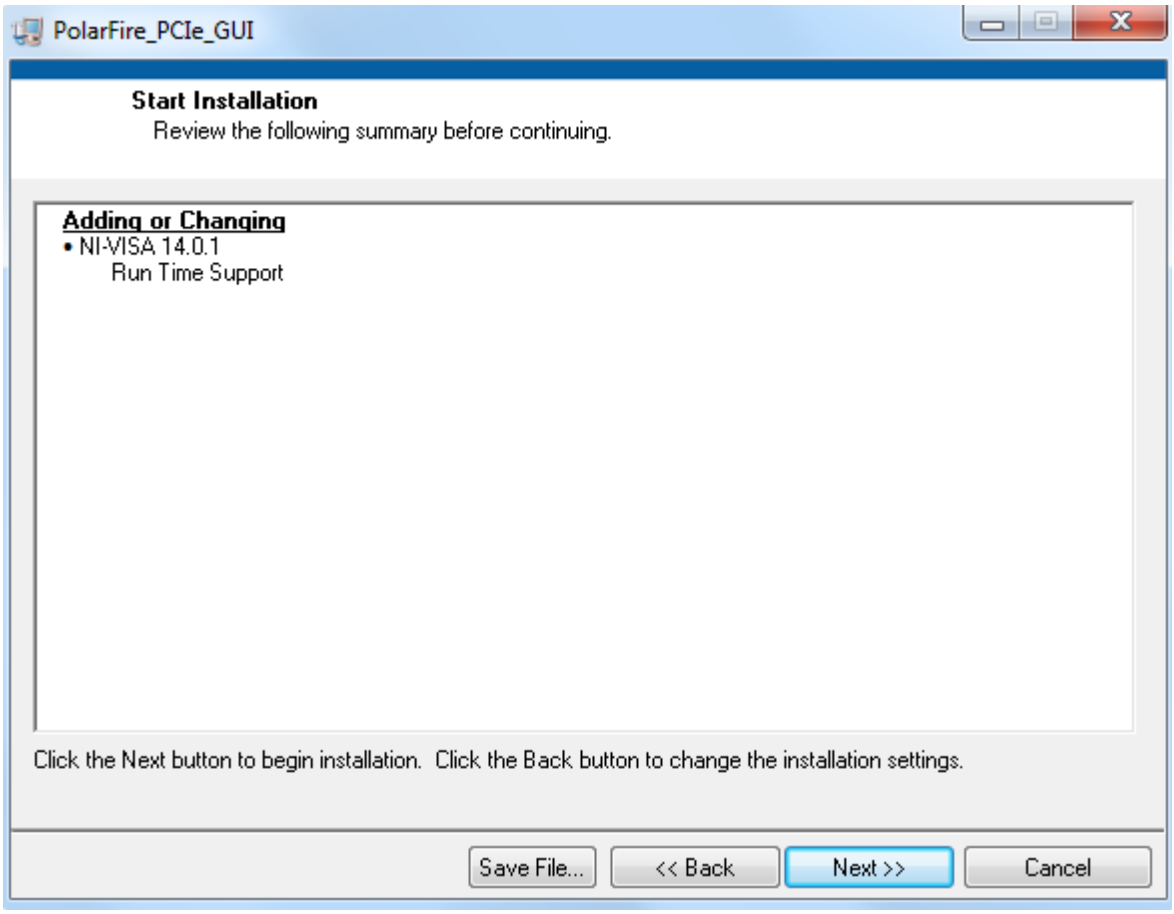


Figure 23: PCIe Demo Application Installing Steps

5. Click **Finish** to complete the installation.

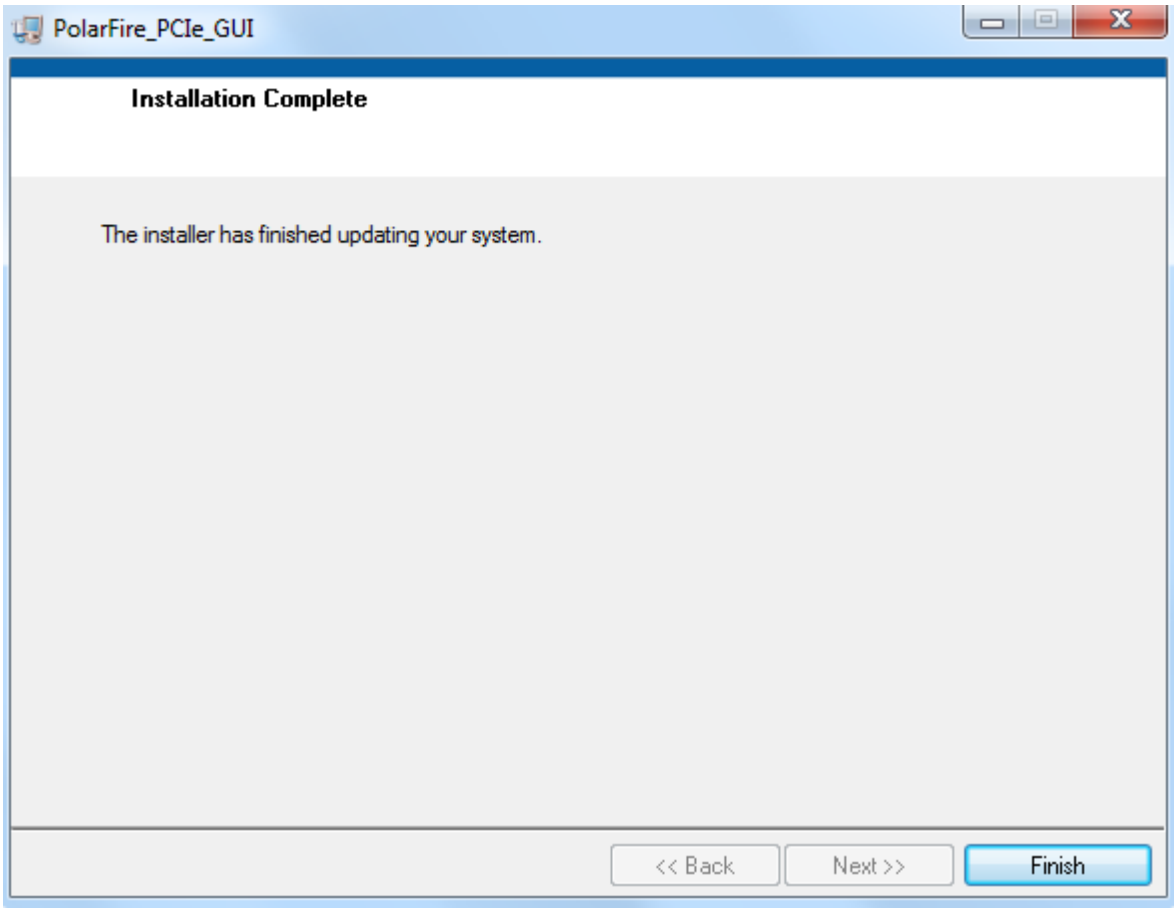


Figure 24: Running the Demo - Successful Installation of PCIe Demo Application

4.2 Running the demo through PCIe

This section shows how to connect the board to host PC PCIe slot, installing the PCIe drivers and running the demo application.

4.2.1 Connection the Everest DEV Board to the host PC PCIe slot

1. After successful programming, power OFF the Everest DEV Board and shut down the host PC[2].
2. Insert the Everest DEV Board in a free PCIe slot of the host PC. The slot must have at least 4 lanes. This demo is designed to work with any PCIe Gen 2 compliant slot. If the host PC does not support Gen 2 compliant slot, the demo switches to Gen 1 mode.
3. Power on the power supply switch **K2**[3].
4. Power on the host PC.
5. After the operating system is loaded check the **Device Manager** of the host PC for the PCIe device.

[2] If the PC is not powered OFF, the PCIe device detection and the selection of Gen1 or Gen2 mode may fail. PCIe hor

[3] If the PC was shut down, but the power supply is not switched off, the PC may power on without manually pressing the power button.

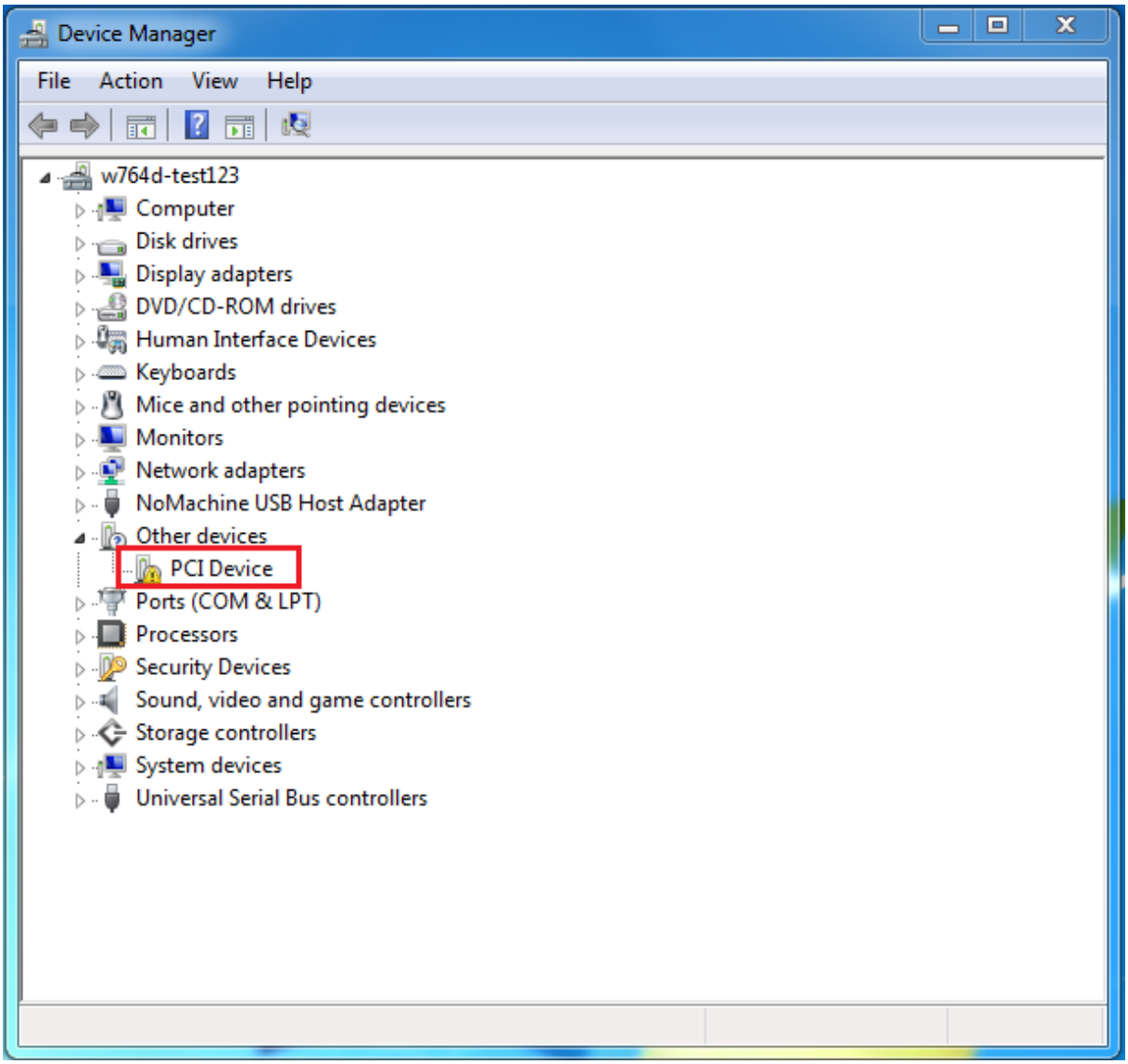


Figure 25: Running the Demo - Device Manager

4.2.2 Driver Installation

Perform the following steps to install the PCIe drivers on the host PC:

1. Right-click **PCI Device** in the **Device Manager** and select **Update Driver Software...** as shown in **Fehler! Verweisquelle konnte nicht gefunden werden.**. To install the drivers, administrative rights are required.
2. In the **Update Driver Software - PCIe Device** window, select **Browse my computer for driver software** as shown in Figure 26.
3. Browse the driver's folder and click **Next** as shown in Figure 27: mpf_dg0756_liberosocpolarfirev2p1_df\PCIe_Drivers\Win_64bit_PCIe_Driver.
4. The **Windows Security** dialog box is displayed. Click **Install** as shown in the following figure. After successful driver installation, a message appears. See Figure 28.

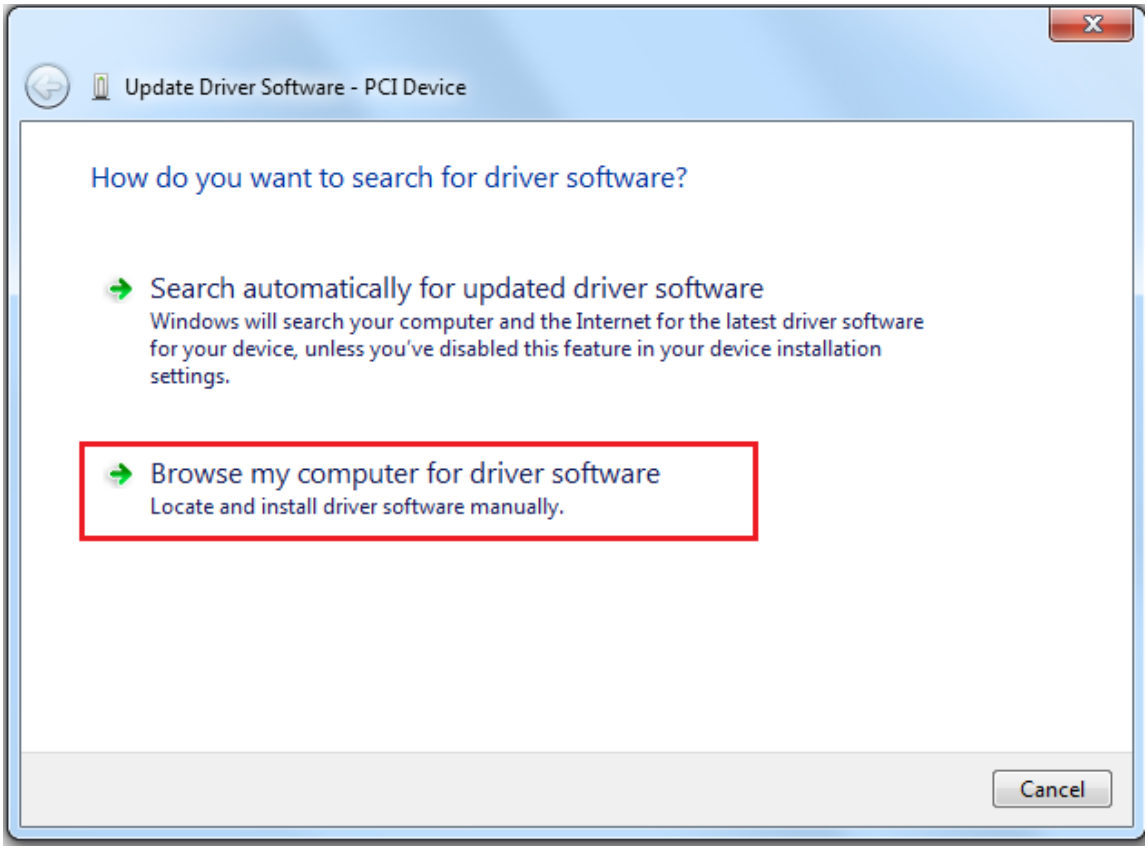


Figure 26: Driver Installation - Browse for Driver Software

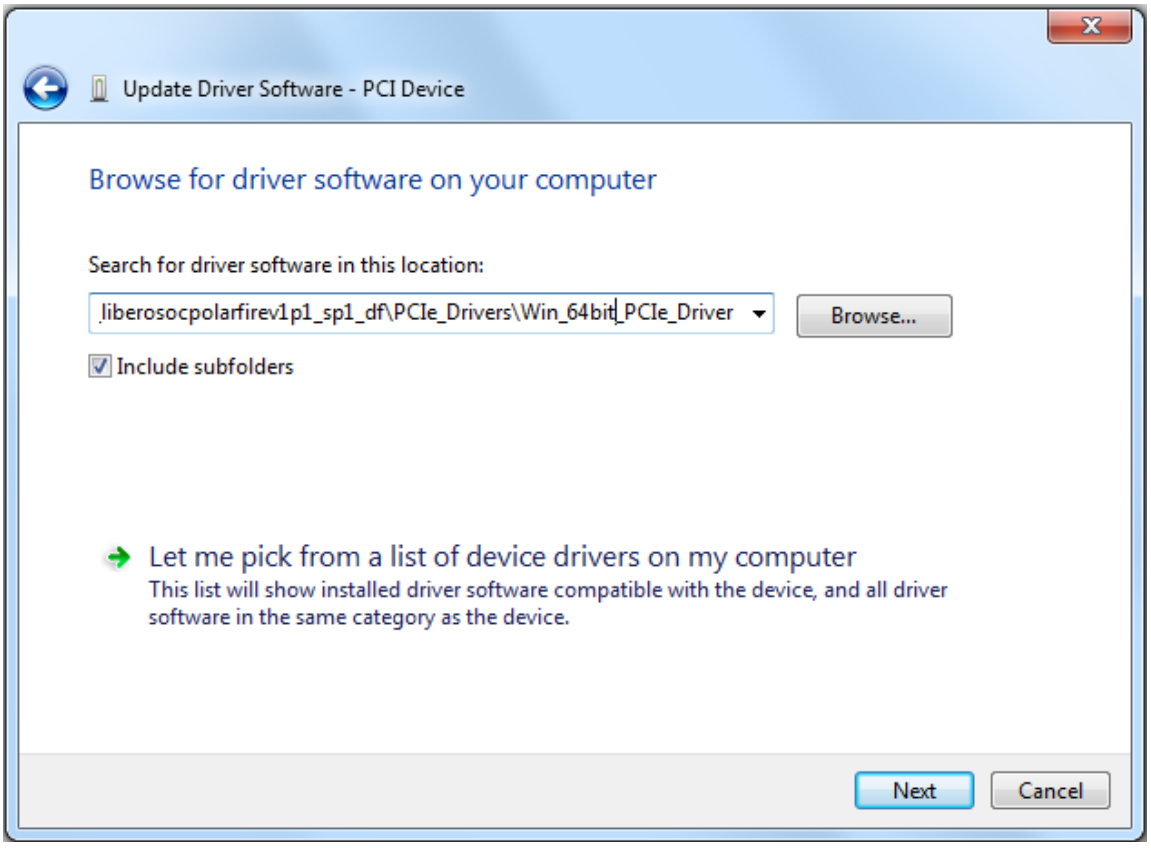


Figure 27: Driver Installation - Browse for Driver Software cont.

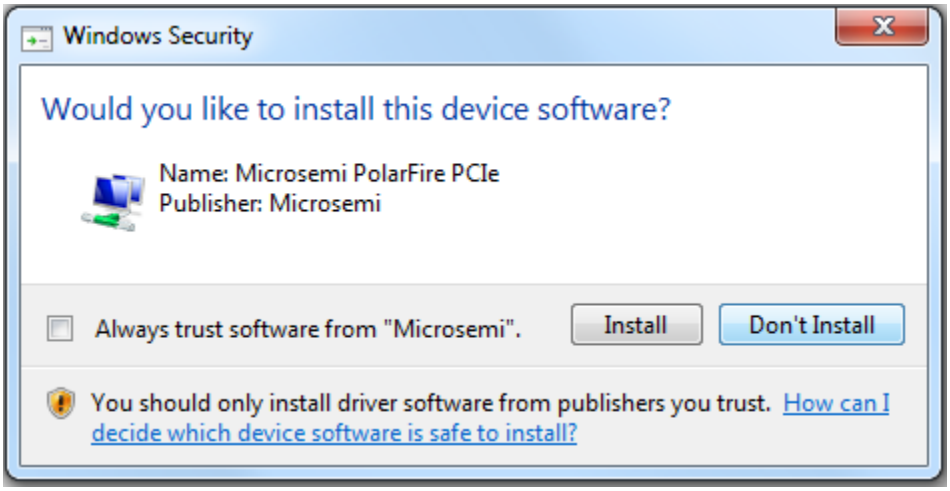


Figure 28: Driver Installation - Windows Security

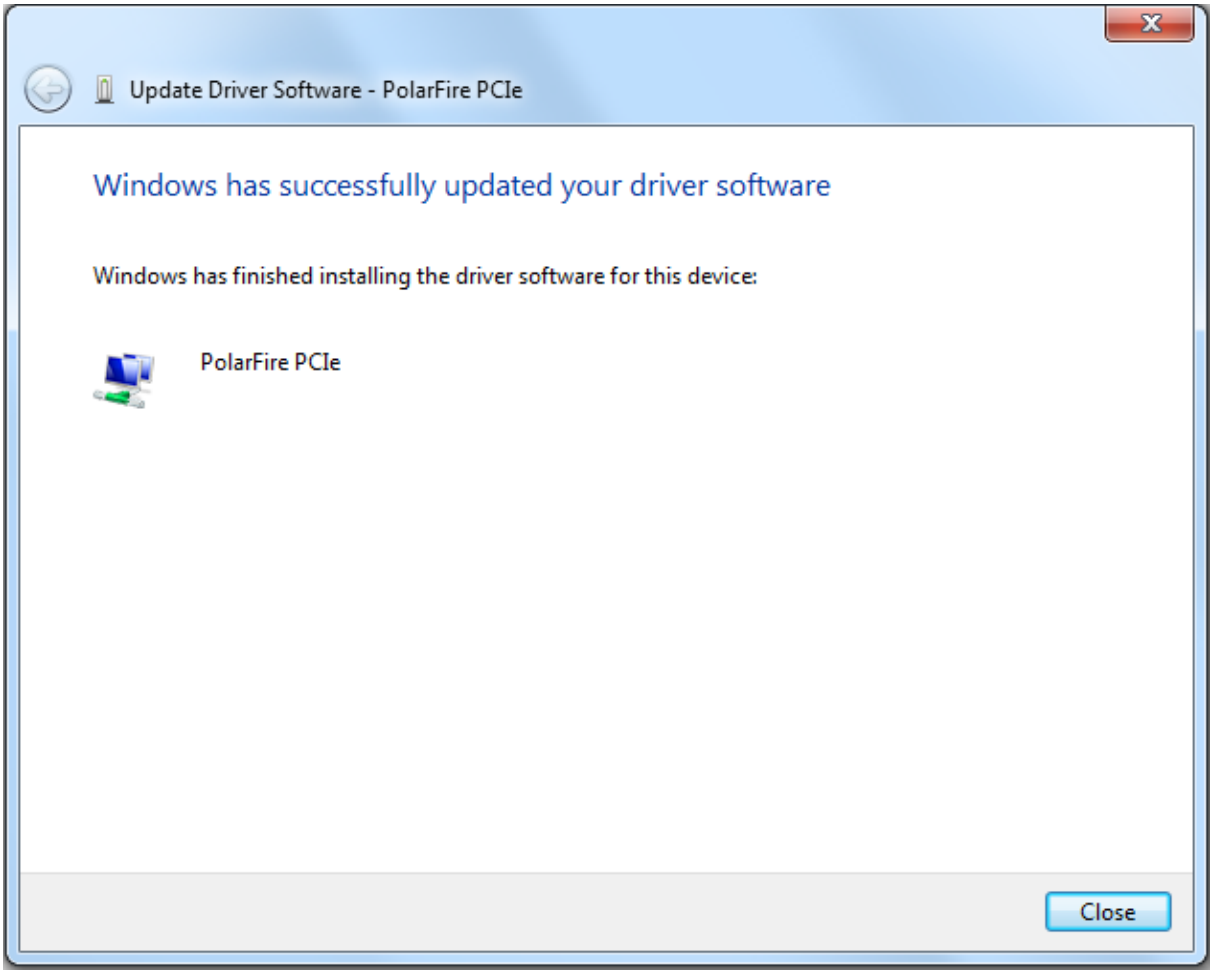


Figure 29: Driver Installation - Successful Driver Installation

4.2.3 Running the PCIe Demo Application

The following steps describe how to run the demo design:

1. Click to expand the **PolarFire PCIe** device in the host PC **Device Manager** as shown in Figure 30.
2. Go to **All Programs > PolarFire_PCIe_GUI > PolarFire_PCIe_GUI**. The **PolarFire PCIe Demo** window is displayed as shown in Figure 31.
3. Click **Connect**. The application detects and displays the information related to the connected kit such as Device Vendor ID, Device Type, Driver Version, Driver Time Stamp, Demo Type, Supported Link Width, Negotiated Link Width, Supported Speed, Negotiated Speed, Number of Bars, and BAR Address as shown in Figure 32.
4. Click the **Demo Controls** tab to display the **LED Controls**[4], **DIP Switch Status**[5], and **Interrupt Counters** as shown in Figure 33.
5. Click Start **LED ON/OFF Walk** and **Enable Interrupt Session** to view the controlling LEDs and monitoring the interrupts simultaneously as shown in Figure 34.
6. Click the **Config Space** tab to view the details about the PCIe configuration space as shown in Figure 35.
7. Click the **PCIe Read/Write** tab to perform read and write operations to DDR/LSRAM using BAR2 space.
8. Click **Read** to read the 4 KB memory mapped to BAR2 space for DDR and LSRAM as shown in Figure 36 to Figure 38.
9. Click the **DMA Operations** tab for different DMA operations such as DDR and LSRAM.

[4] Because the Everest DEV Board only has 4 LEDs, there will be a little pause while the demo application turns on LED 5 to 8.
[5] There are no DIP switches on the Everest DEV Board.

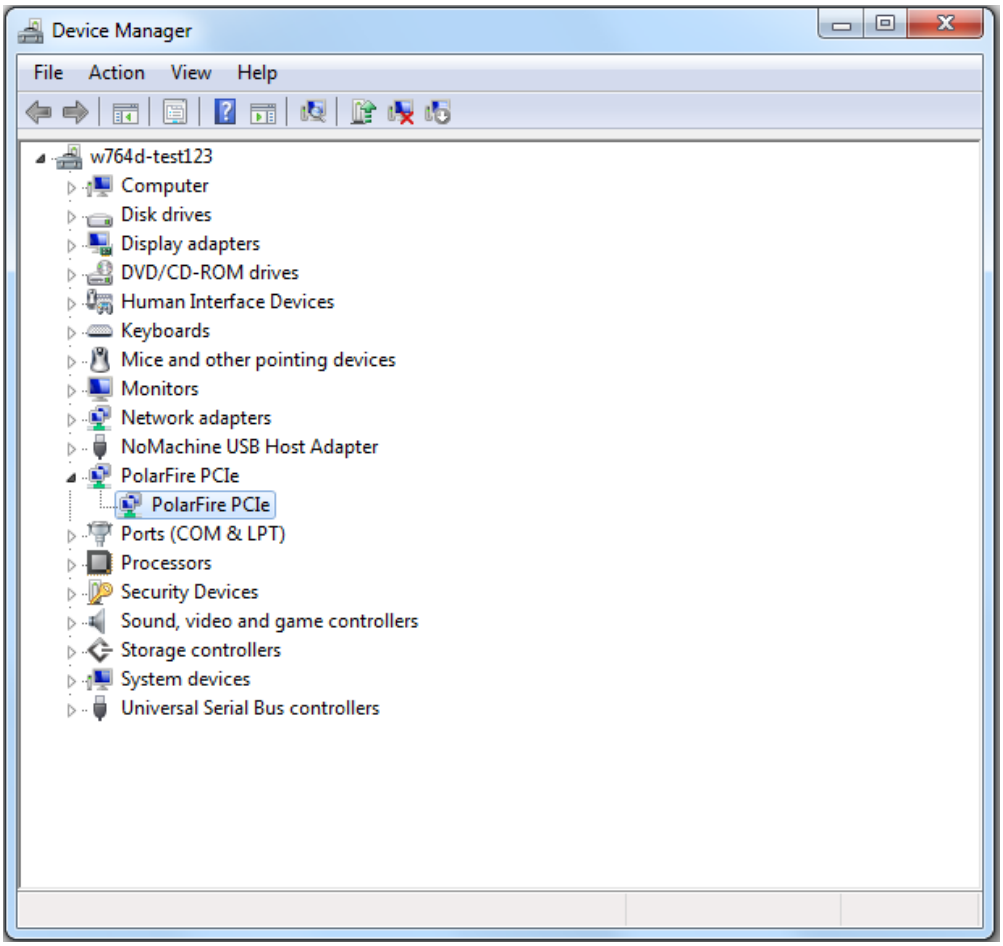


Figure 30: Device Manager - PolarFire PCIe device detected

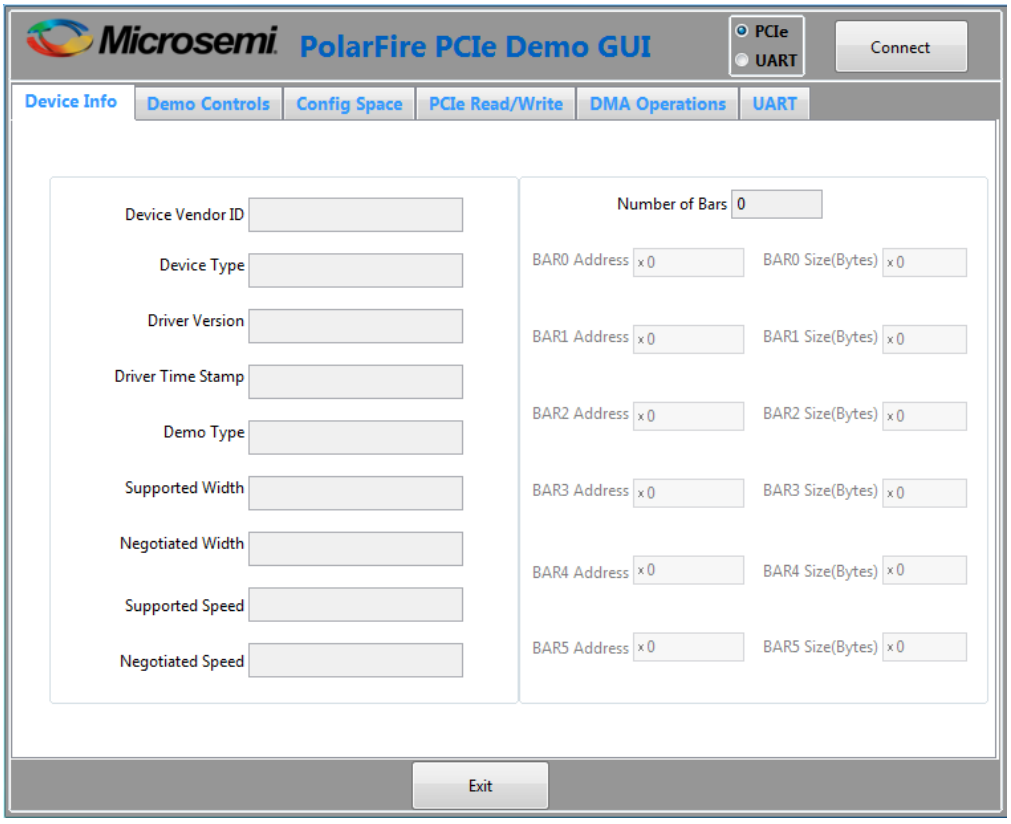


Figure 31: PCIe end point demo application

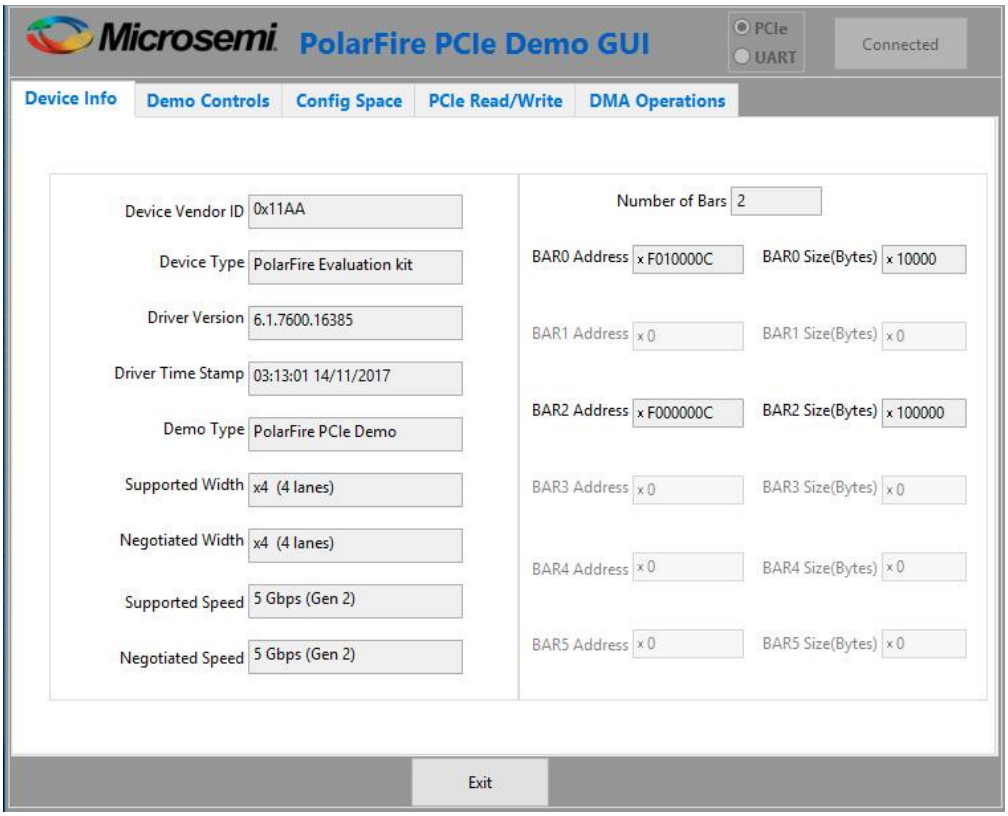


Figure 32: Demo application - Device Info tab

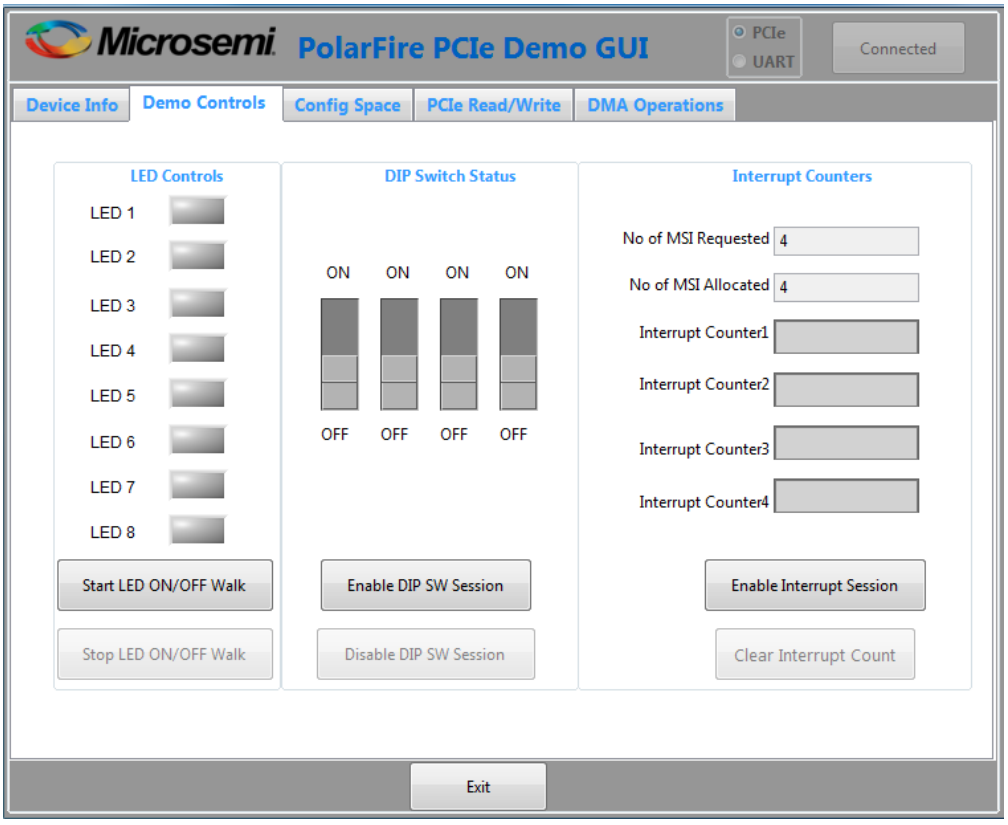


Figure 33: Demo application - Demo Controls tab

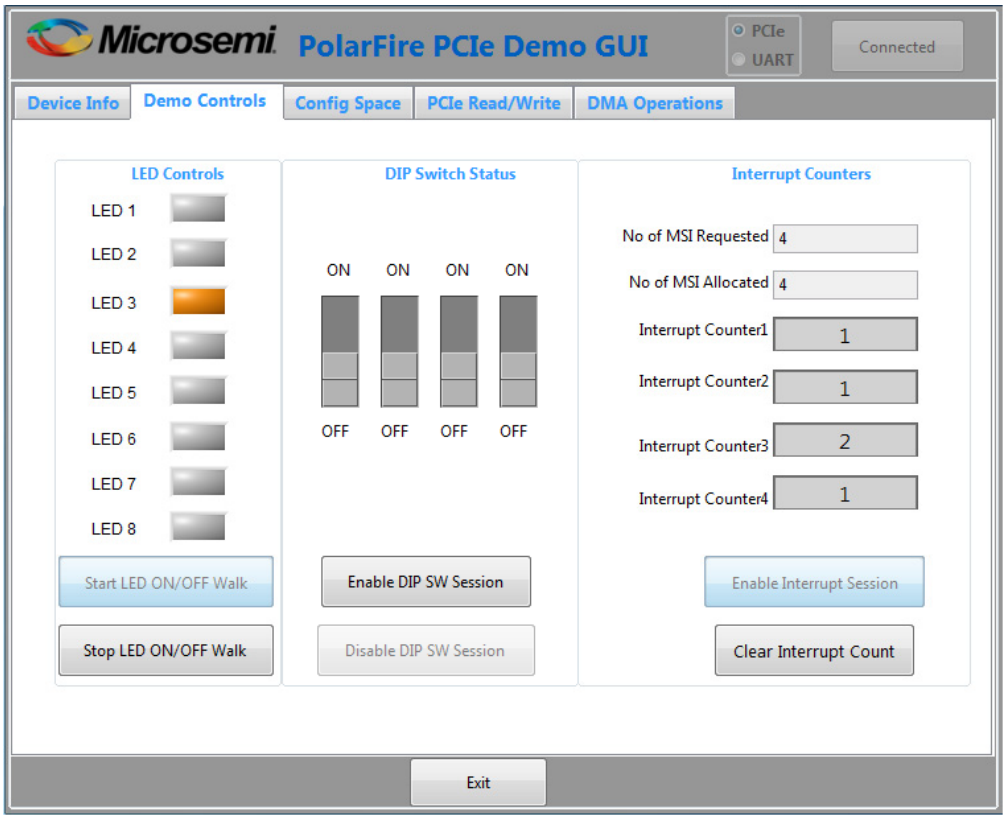


Figure 34: Demo application - Demo Controls tab - LED walk and push button interrupt count

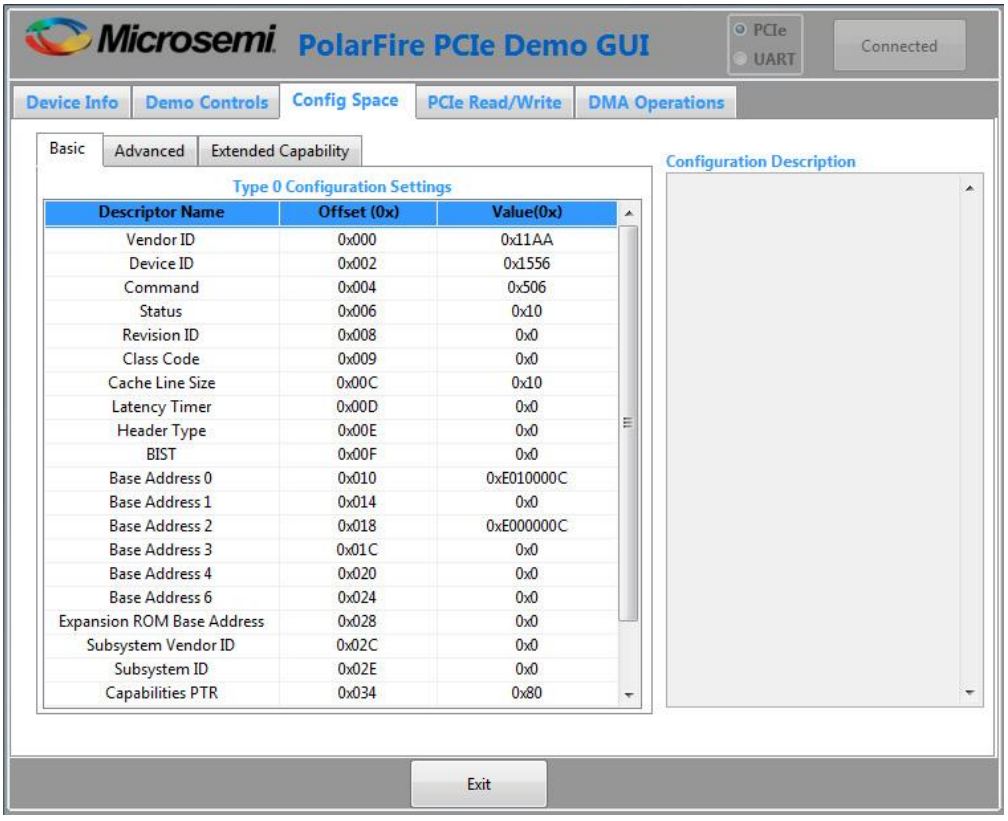


Figure 35: Demo application - Config Space tab

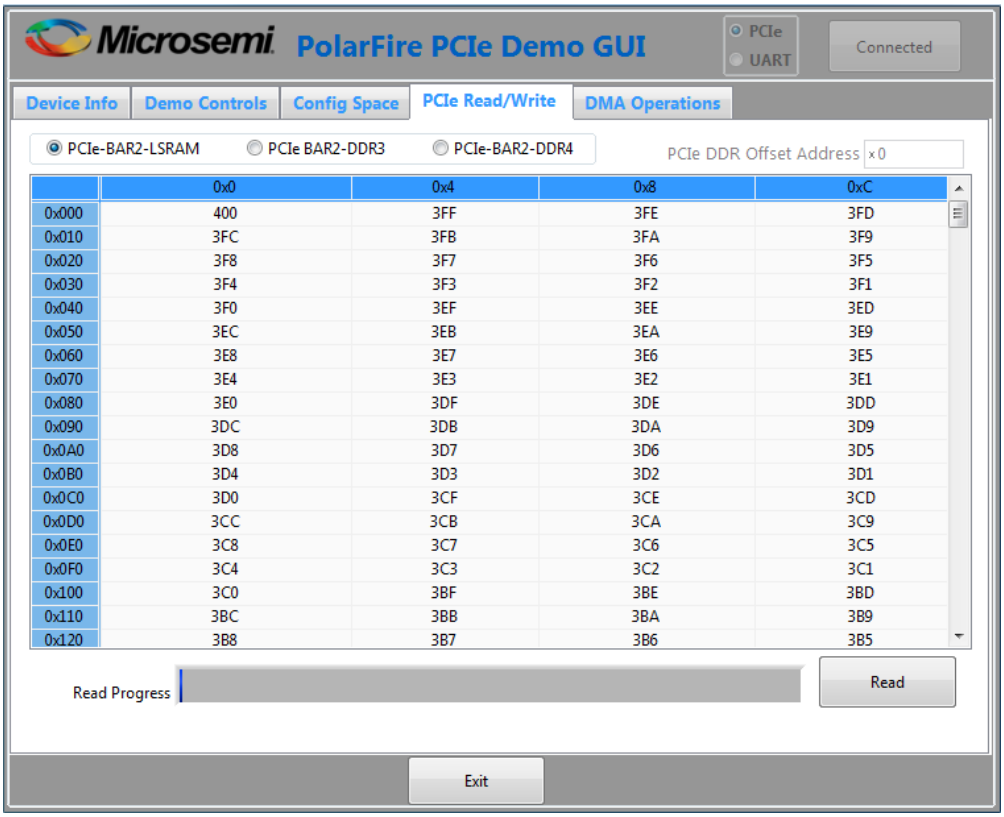


Figure 36: Demo application - PCIe Read/Write tab – LSRAM

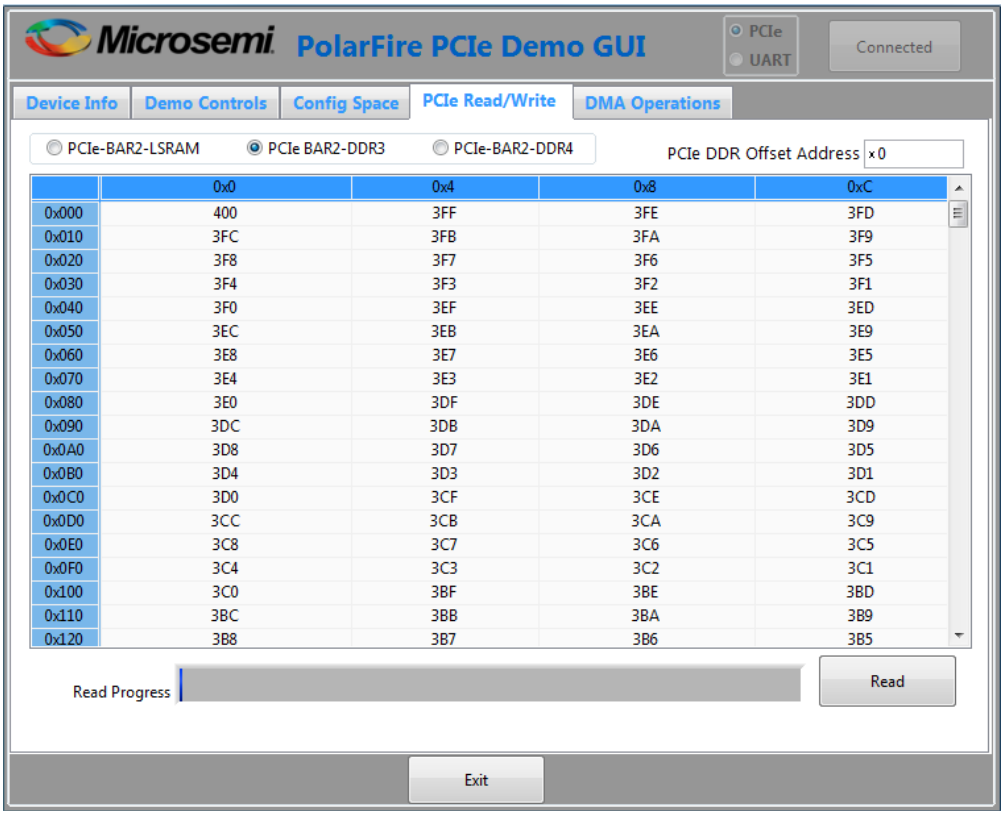


Figure 37: Demo application - PCIe Read/Write tab - DDR3 16 Bit

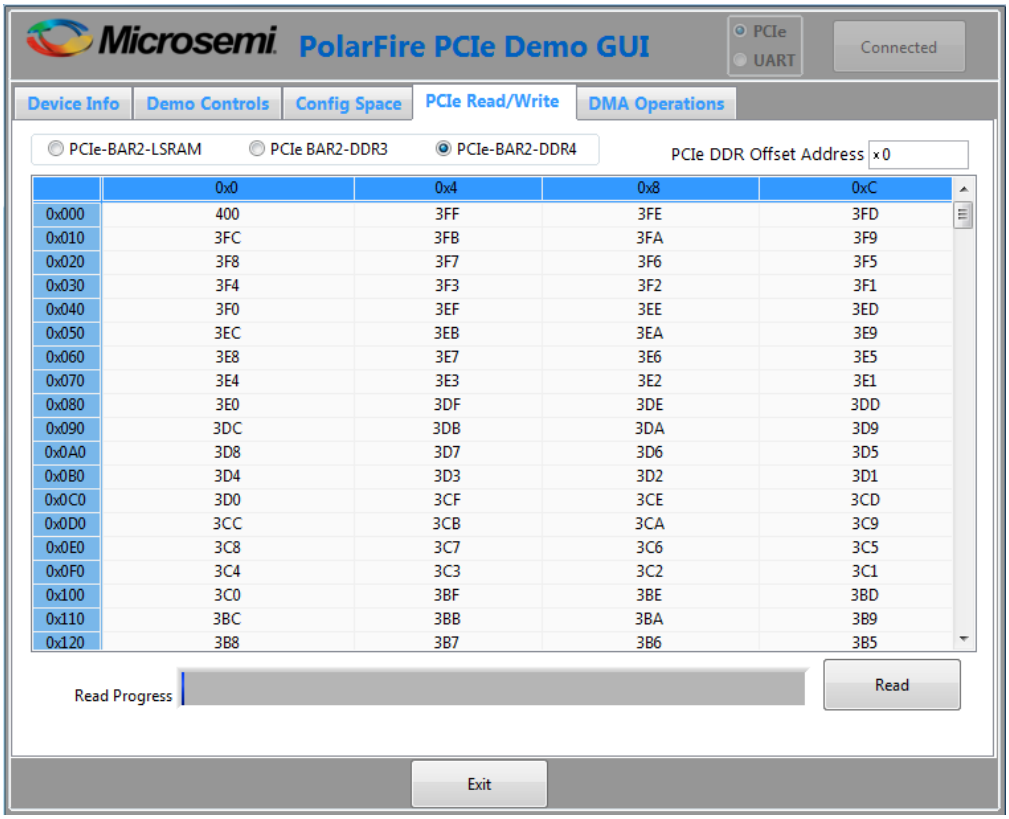


Figure 38: Demo application - PCIe Read/Write tab - DDR3 32 Bit

4.2.3.1 Continuous DMA Operations

The following instructions describe running DMA operations between PC and DDR3 16 Bit, PC and DDR3 32 Bit and PC and LSRAM:

1. Select one of the following options from the **DMA Transfer Type Selection** drop-down list:
    - **PC->DDR3** - to transfer data from host PC to DDR3 16 Bit memory
    - **DDR3->PC** - to transfer data from DDR3 16 Bit memory to host PC
    - **Both: PC<->DDR3** - to transfer data from host PC to and from DDR3 16 Bit memory
    - **PC->DDR4** - to transfer data from host PC to DDR3 32 Bit memory
    - **DDR4->PC** - to transfer data from DDR3 32 Bit memory to host PC
    - **Both PC<->DDR4** - to transfer data from host PC to and from DDR3 32 Bit memory
    - **PC->LSRAM** - to transfer data from host PC to LSRAM memory
    - **LSRAM->PC** - to transfer data from LSRAM memory to host PC
    - **Both: PC<->LSRAM** - to transfer data from host PC to and from LSRAM memory

2. Select **Transfer Size**[6] (4 KB to 64 KB) from the drop-down list. Maximum contiguous DMA size is 64 KB because the host PC may not have contiguous memory of more than 64 KB. For DMA operations that require more than 64 KB, use SGDMA.
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows Continuous DMA Operations.

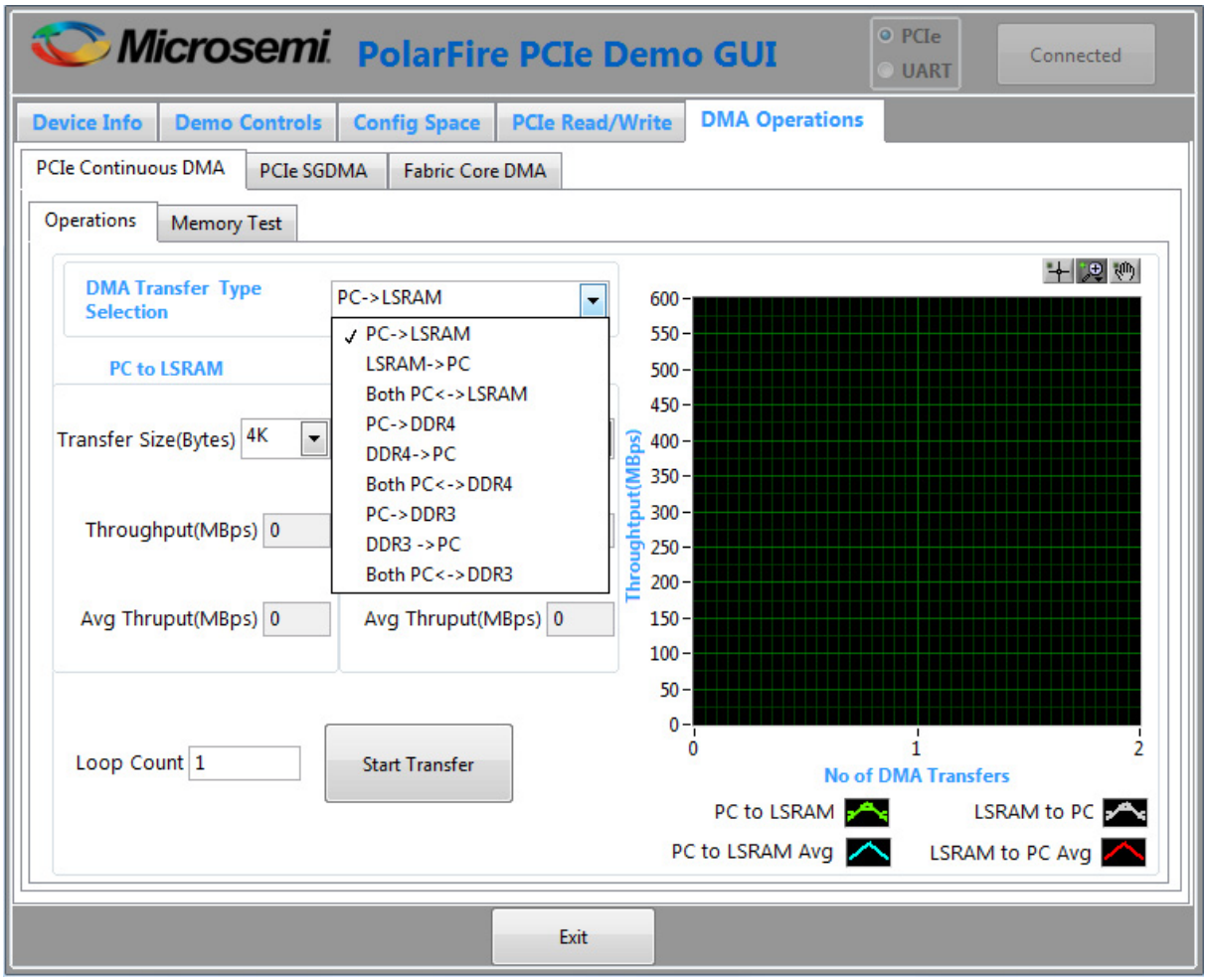


Figure 39: Demo application - continuous DMA operations

[6] The AXI LSRAM in the design is configured for 4 kB. This 4 kB is over written if more than 4 kB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

The following figure shows the throughput and average throughput in MBps.

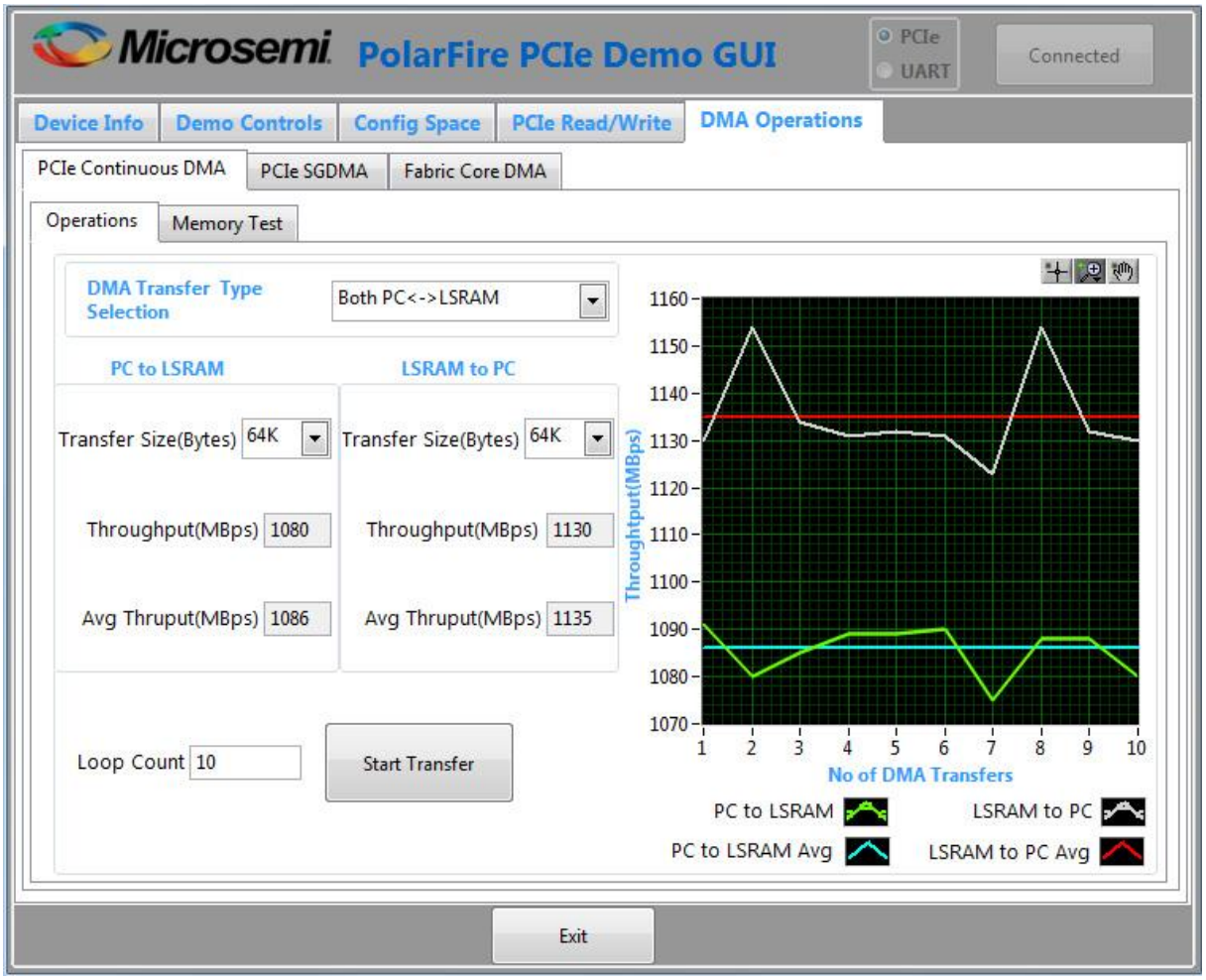


Figure 40: Demo application - continuous DMA from PC to LSRAM and vice versa

4.2.3.2 Continuous DMA – Memory Test

The following instructions describe running **Memory Test** between PC and DDR3 16 Bit, DDR3 32 Bit and LSRAM:

1. Select one of the following options from the Test Selection drop-down list:
    - **PC<->DDR3** - to transfer data from host PC to and from DDR3 16 Bit memory
    - **PC<->DDR4** - to transfer data from host PC to and from DDR3 32 Bit memory
    - **PC<->LSRAM** - to transfer data from host PC to and from LSRAM memory
2. Select **Transfer Size** (4 kB to 64 kB) from the drop-down list.
3. Select **Pattern Selection** from the drop-down list (Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's).
4. Click **Start**. GUI performs the following task:
    - The host PC creates a buffer and initializes the memory
    - Initiates the PC to DDR DMA
    - Erases the PC buffer

- Initializes the DDR to PC DMA
- Compares the memory against expected memory

The following figure shows Continuous DMA - Memory Test tab.

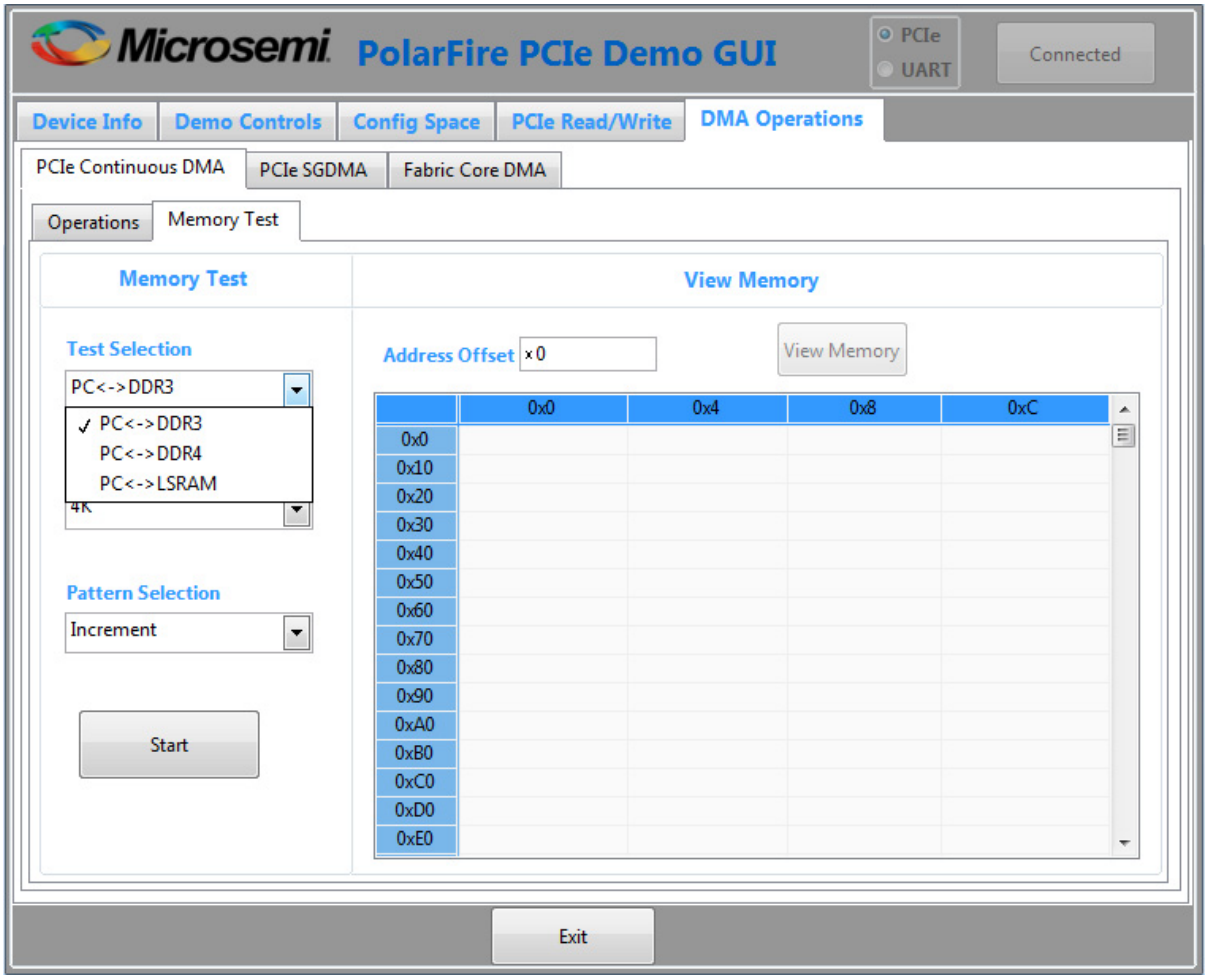


Figure 41: Demo application – Continuous Memory Test – Transfer Type Selection

Memory Test Successful window appears, as shown in the following figure.

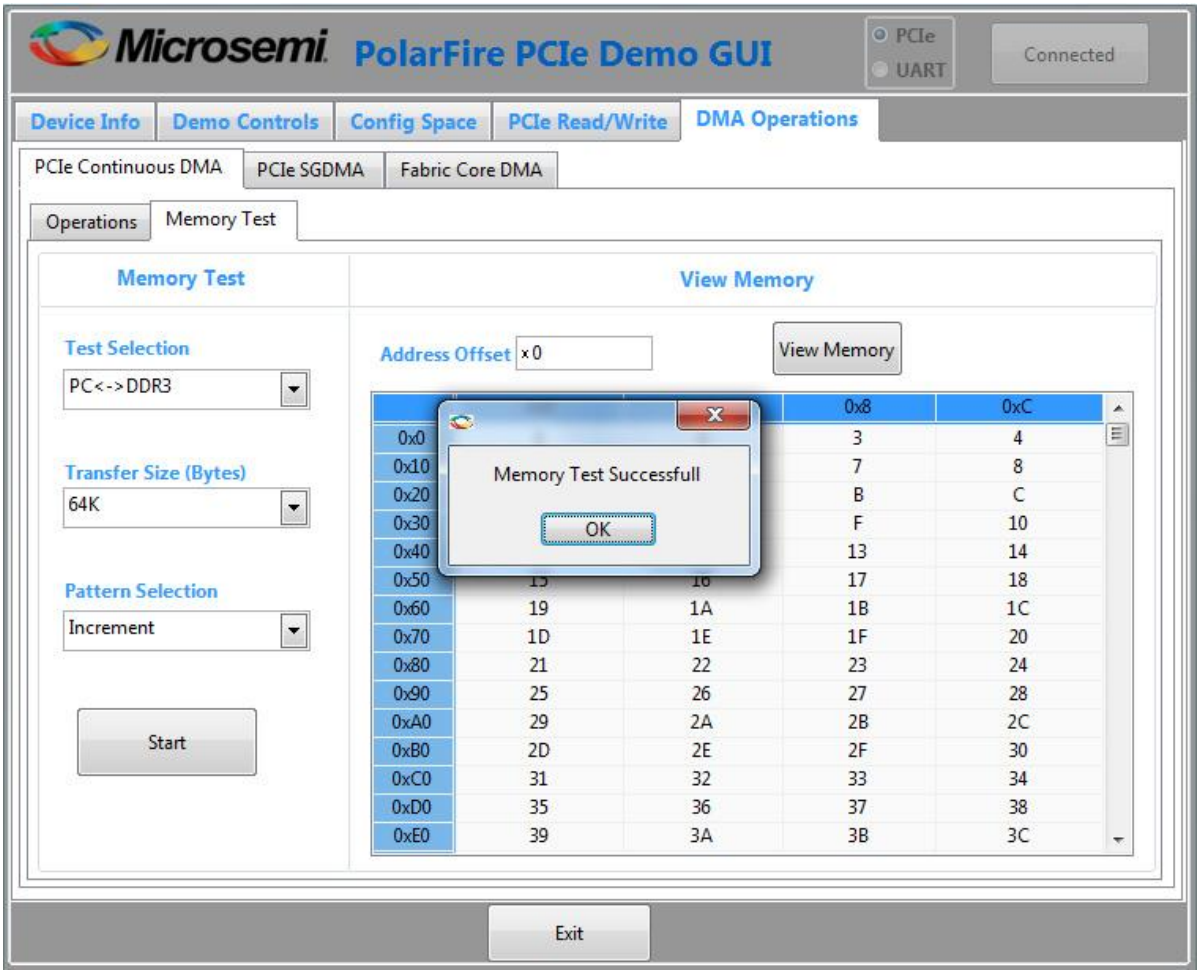


Figure 42: Demo application - Continuous DMA Memory Test - Memory Test Successful

If memory test fails, the GUI displays the first failed memory location. Change the **Offset Address** and click **View Memory** to read the RAM memory content.

4.2.3.3 SGDMA Operations

The following instructions describe running SGDMA operations between PC and DDR3 16 Bit, PC and DDR3 32 Bit:

1. Select one of the following options from the **DMA Transfer Type Selection** drop-down list:
    - **PC -> DDR3** - to transfer data from host PC to DDR3 16 Bit memory
    - **DDR3 -> PC** - to transfer data from DDR3 16 Bit memory to host PC
    - **Both: PC <-> DDR3** - to transfer data from host PC to and from DDR3 16 Bit memory
    - **PC -> DDR4** - to transfer data from host PC to DDR3 32 Bit memory
    - **DDR4 -> PC** - to transfer data from DDR3 32 Bit memory to host PC
    - **Both: PC <-> DDR4** - to transfer data from host PC to and from DDR3 32 Bit memory

2. Select **Transfer Size** (4 kB to 64 kB) from the drop-down list.
3. Enter the **Loop Count** in the box. The **Buffer Descriptors** show the number of descriptors created by the host driver for each SGDMA operation.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows the SGDMA Operations.

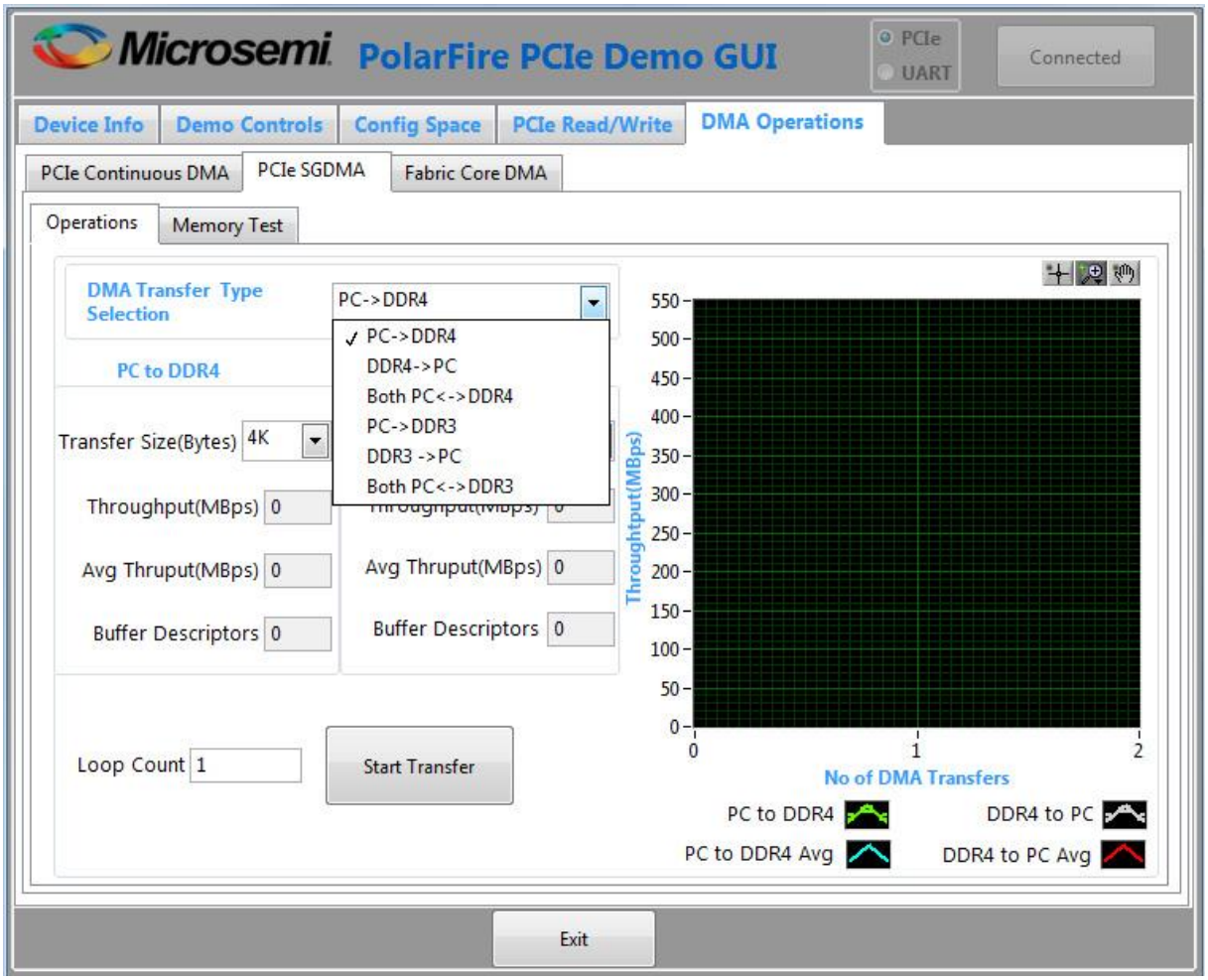


Figure 43: Demo application - SGDMA operations

4.2.3.4 SGDMA Memory Test

The following instructions describe running **Memory Test** between PC and DDR3 16 Bit, DDR3 32 Bit and LSRAM:

1. Select one of the following options from the **Test Selection** drop-down list:
   - **PC <-> DDR3** - to transfer data from host PC to and from DDR3 16 Bit memory
   - **PC <-> DDR4** - to transfer data from host PC to and from DDR3 32 Bit memory
2. Select **Transfer Size** (4 kB to 1 MB) from the drop-down list.
3. Select **Pattern Selection** from the drop-down list (Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's).

4. Click **Start**. GUI performs the following task:
    - The host PC creates a buffer and initializes the memory
    - Initiates the PC to DDR DMA
    - Erases the PC buffer
    - Initializes the DDR to PC DMA
    - Compares the memory against expected memory
5. Click **OK**.
6. Change the **Offset Address** and click **View Memory** to read the RAM memory content.

The following figure shows SGDMA Memory Test tab.

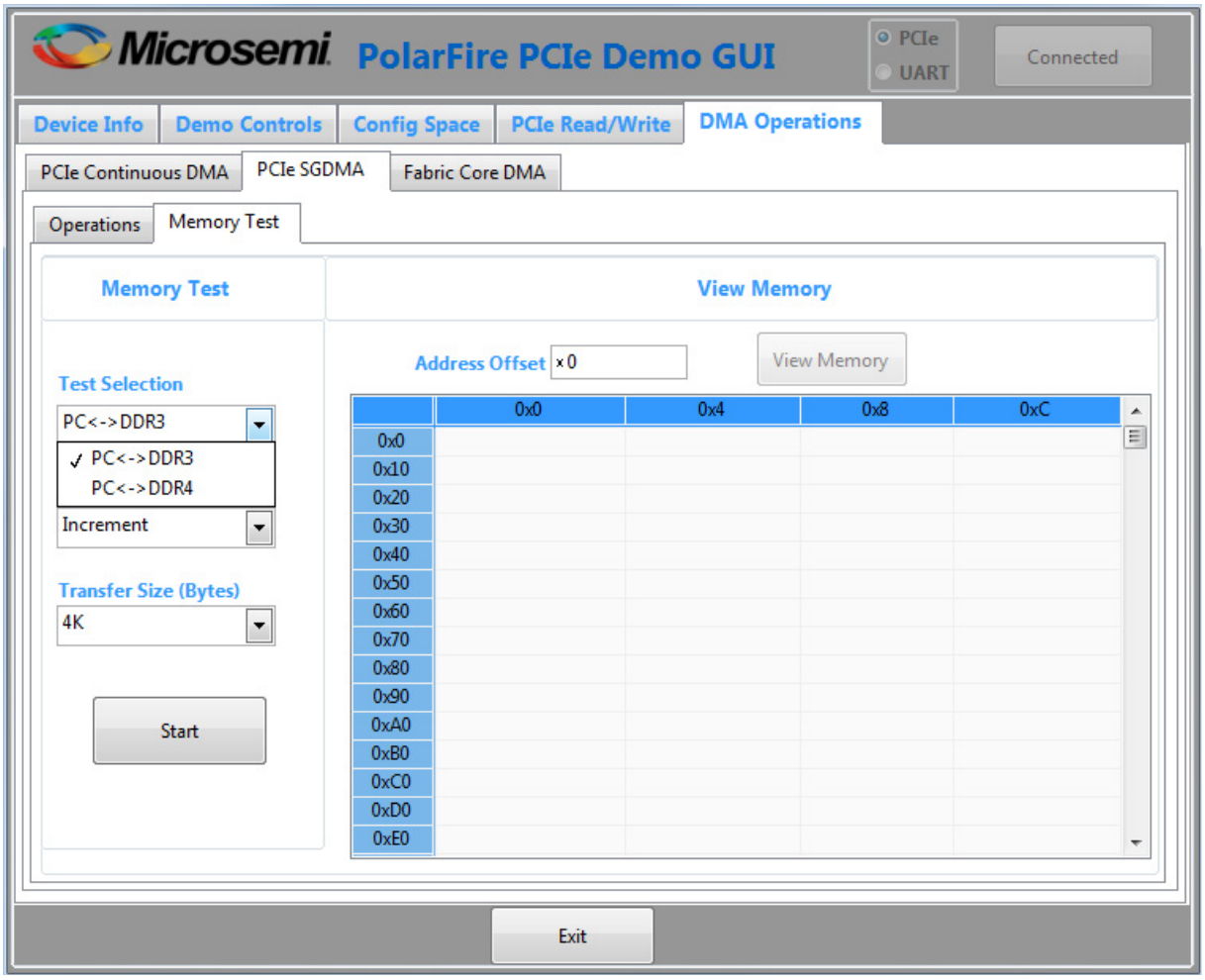


Figure 44: Demo application - SGDMA Memory Test tab

Memory Test Successful window appears, as shown in the following figure.

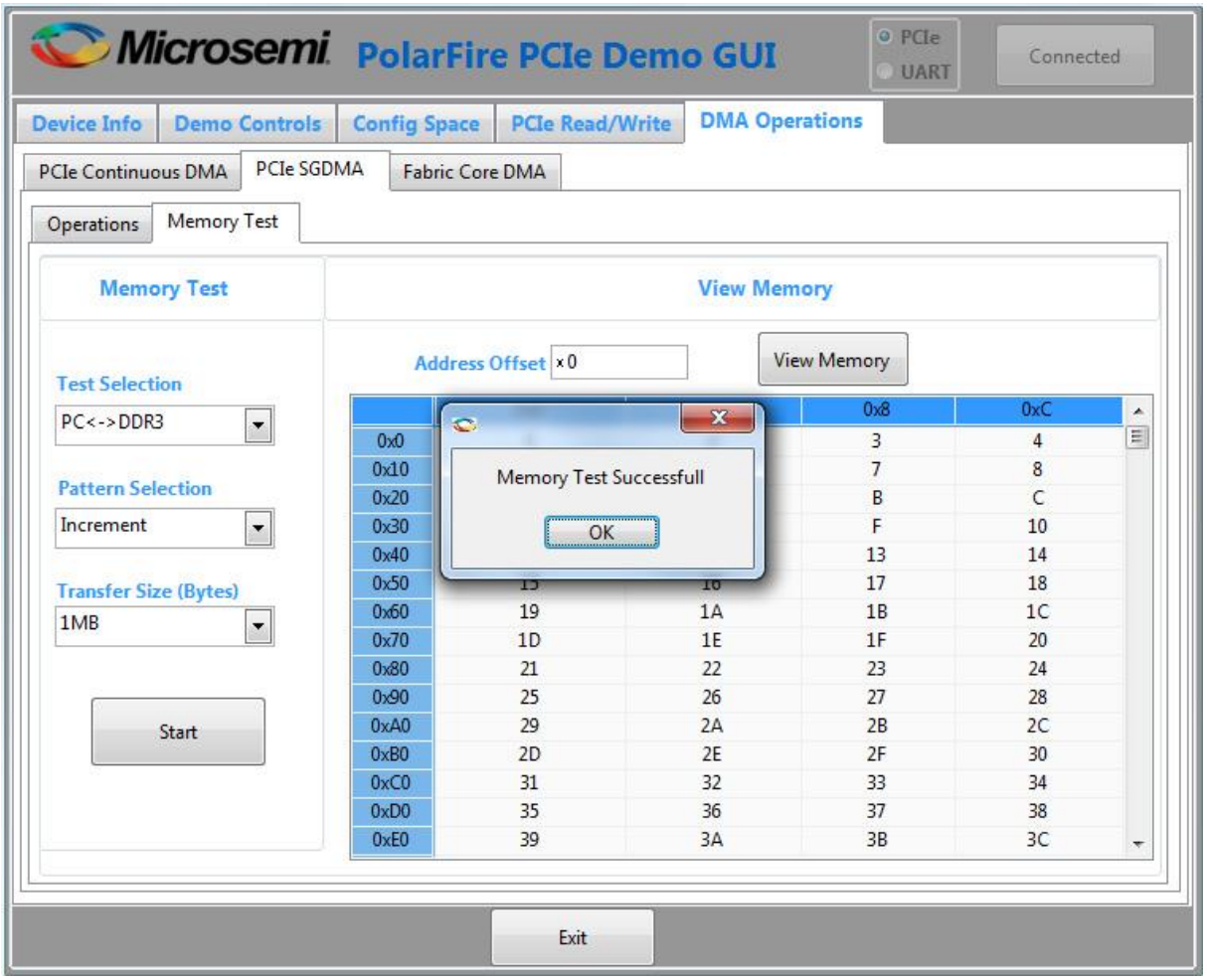


Figure 45: Demo application - SGDMA Memory Test Successful

4.2.3.5 Core DMA Operations

The following instructions describe running DMA operations between LSRAM and DDR3 16 Bit, LSRAM and DDR3 32 Bit, DDR3 16 Bit and DDR3 32 Bit:

1. Select one of the following options from the **DMA Transfer Type Selection** drop-down list:
   - **LSRAM -> DDR3** - to transfer data from LSRAM to DDR3 16 Bit memory
   - **DDR3 -> LSRAM** - to transfer data from DDR3 16 Bit memory to LSRAM
   - **Both: LSRAM <-> DDR3** - to transfer data from LSRAM to and from DDR3 16 Bit memory
   - **LSRAM -> DDR4** - to transfer data from LSRAM to DDR3 32 Bit memory
   - **DDR4 -> LSRAM** - to transfer data from DDR3 32 Bit memory to LSRAM
   - **Both: LSRAM <-> DDR4** - to transfer data from LSRAM to and from DDR3 32 Bit memory
   - **DDR4 -> DDR3** - to transfer data from DDR3 32 Bit to DDR3 16 Bit memory
   - **DDR3 -> DDR4** - to transfer data from DDR3 16 Bit to DDR3 32 Bit memory

- **Both: DDR4 <-> DDR3** - to transfer the data from DDR3 32 Bit to and from DDR3 16 Bit memory

2. Select **Transfer Size**[7] (4 kB to 1 MB) from the drop-down list.
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows Core DMA Operations.
5. Click **Exit** to quit the demo.

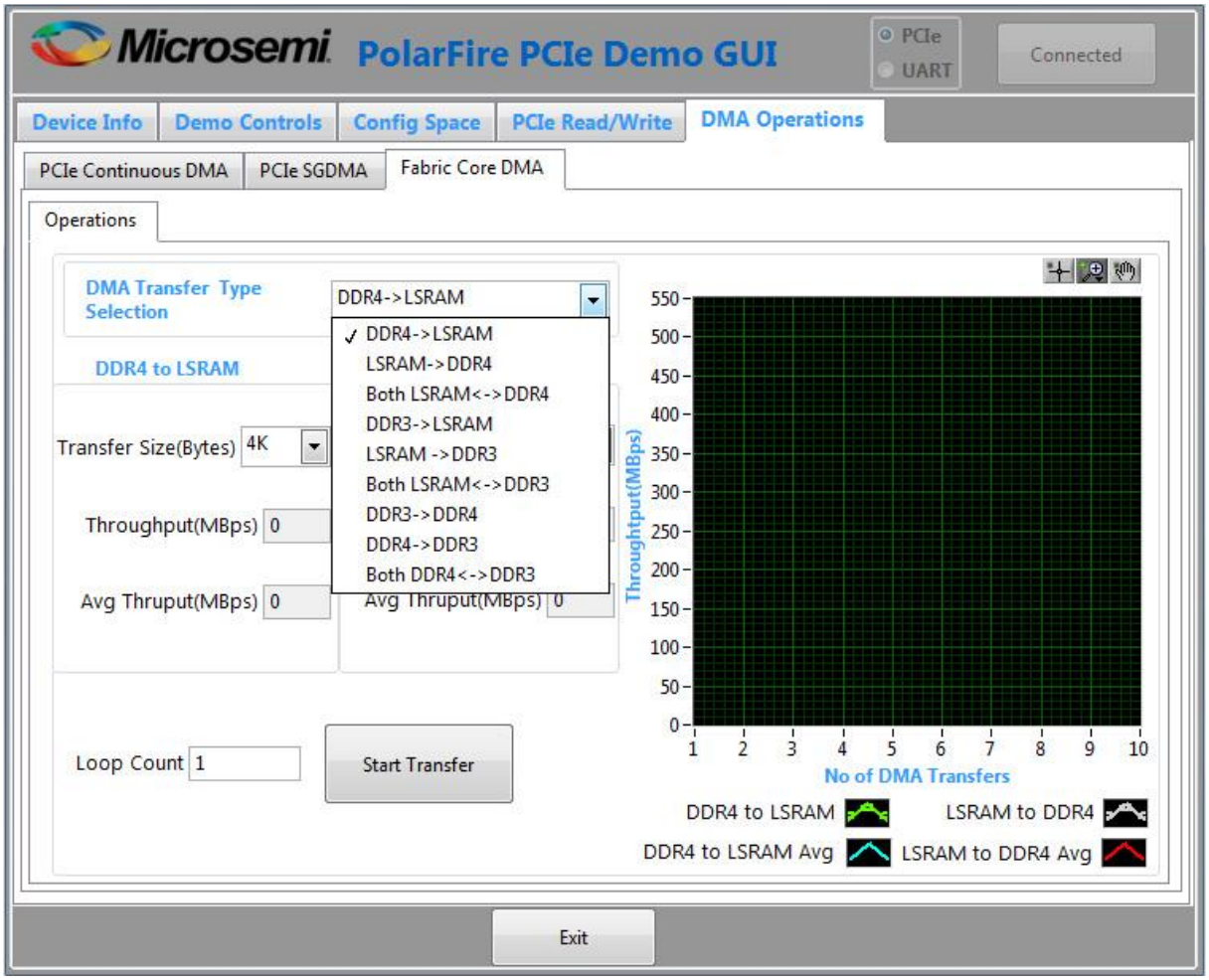


Figure 46: Demo application - Core DMA operations

[7] The AXI LSRAM in the design is configured for 4 kB. This 4 kB is over written if more than 4 kB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

4.3 Running the demo through UART

If no PCIe slot is available, onboard DMA and memory test could be done by the demo application using the USB UART interface of the Everest DEV Board. The COM port number of the USB UART interface will be set by the operating system after installation. Checking the COM ports with the **Device Manager** will give a similar result like in the following figure.

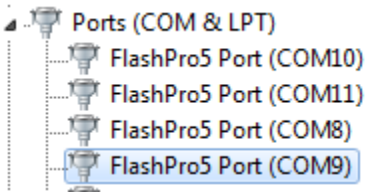


Figure 47: Device Manager - COM ports

The following steps describe how to run the reference design using the USB UART interface:

1. Go to **All Programs > PolarFire_PCIe_GUI > PolarFire_PCIe_GUI**. The **PolarFire PCIe Demo** window is displayed as shown in Figure 48.
2. Select the **UART** radio button and click **Connect**. The GUI application scans for UART port and after successful connection, displays the DMA Operations UART tab as shown in Figure 49, page 48.

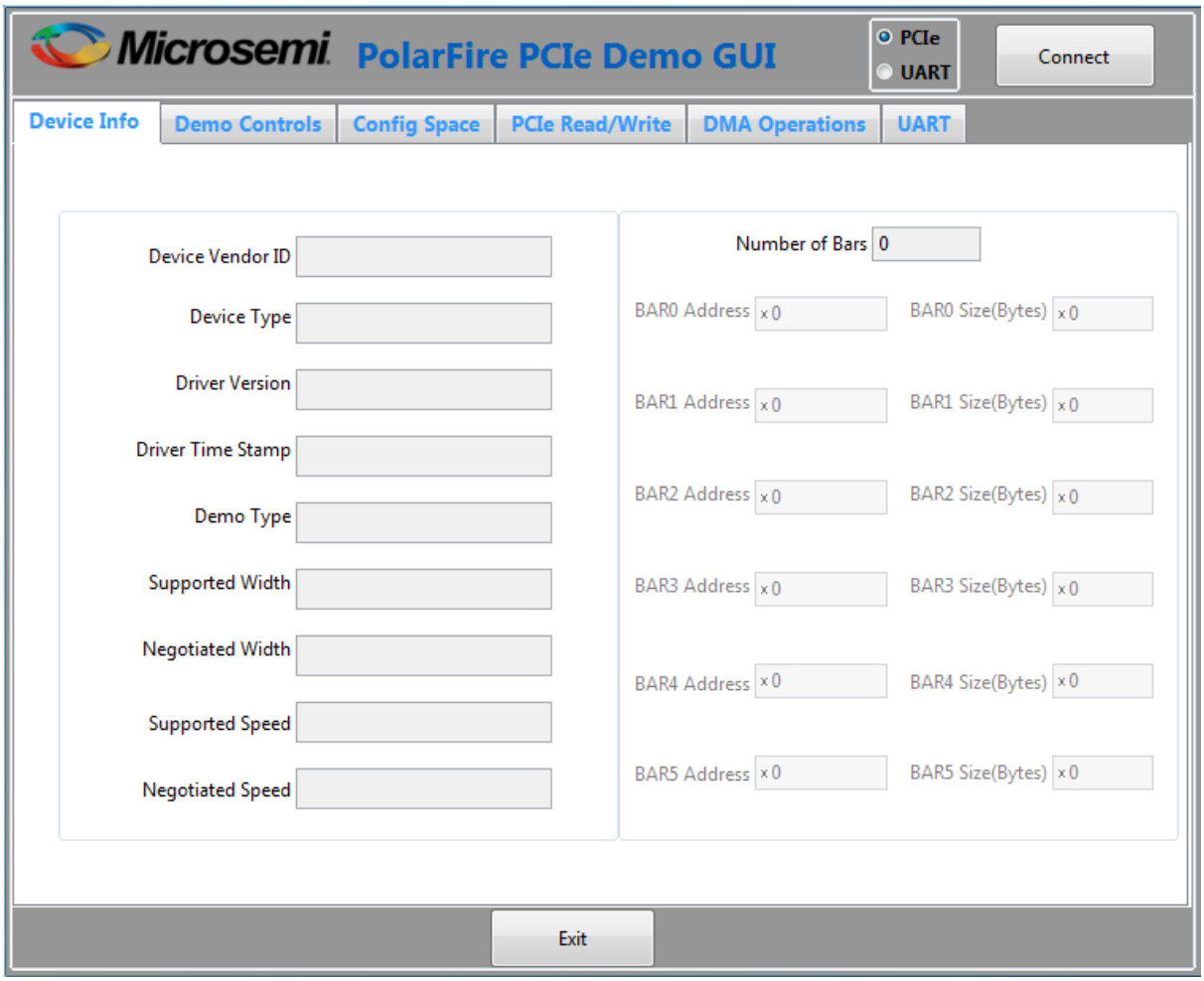


Figure 48: PCIe end point demo application

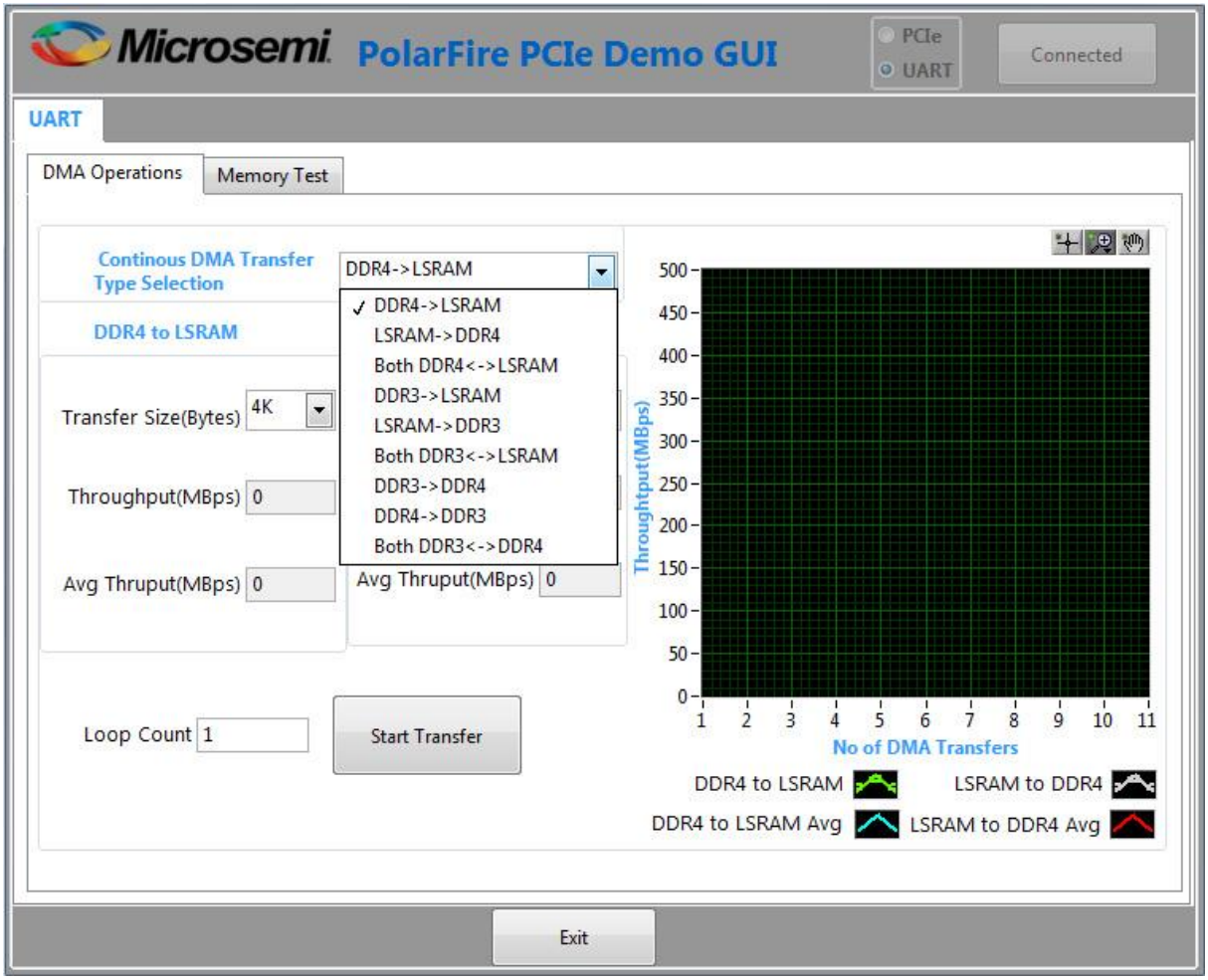


Figure 49: Demo application - UART DMA operations

The following instructions describe the different ways to read data through LSRAM and DDR:

1. Select one of the following options from the Continuous DMA Transfer Type Selection drop-down list:
   - **DDR3 -> LSRAM** - transfer data from DDR3 16 Bit to LSRAM memory.
   - **LSRAM -> DDR3** - transfer data from LSRAM to DDR3 16 Bit memory.
   - **Both: DDR3 <-> LSRAM** - transfer data from DDR3 16 Bit to and from LSRAM memory.
   - **LSRAM -> DDR4** - transfer data from LSRAM to PolarFire DDR3 32 Bit memory.
   - **DDR4 -> LSRAM** - to transfer data from DDR3 32 Bit to LSRAM memory.
   - **Both: LSRAM <-> DDR4** - transfer data from LSRAM to and from DDR3 32 Bit memory.
   - **DDR4 -> DDR3** - transfer data from DDR3 32 Bit to DDR3 16 Bit memory.
   - **DDR3 -> DDR4** - transfer data from DDR3 16 Bit to DDR3 32 Bit memory.
   - **Both: DDR4 <-> DDR3** - transfer data from DDR3 32 Bit to and from DDR3 16 Bit memory.

- **Both: DDR3 <-> DDR4** - transfer data from DDR3 16 Bit to and from DDR3 32 Bit memory.

2. Select **Transfer Size**[8] (4 kB to 512 kB) from the drop-down lists.
3. Enter the **Loop Count** in the box.
4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows DMA throughput and average throughput from the DDR memory to the LSRAM.

The following instructions describe running **Memory Test** between PC and DDR3 16 Bit, DDR3 32 Bit and LSRAM:

1. Select **Transfer Size** (4 kB to 1 MB) from the drop-down list.
2. Select **Pattern Selection** from the drop-down list (Increment, Decrement, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's). For successful Memory test operation, the **Patter Type for Mem Init** and **Patter Type for Mem Test** should be same.
3. Click **Memory Test**.
    - GUI sends command to fabric logic to initiate the LSRAM, DDR3 16 Bit and DDR3 32 Bit memory.
    - GUI sends command to fabric logic to read and compare LSRAM, DDR3 16 Bit and DDR3 32 Bit memory.
4. Click **View Memory**. It shows 1 kB of RAM memory content.
5. Click **OK**.
6. Change the **Offset Address** and click **View Memory** to read the RAM memory content.
7. Click **Exit** to quit the demo.

[8] The AXI LSRAM in the design is configured for 4 kB. This 4 kB is over written if more than 4 kB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

The following figure shows the UART Memory Test tab.

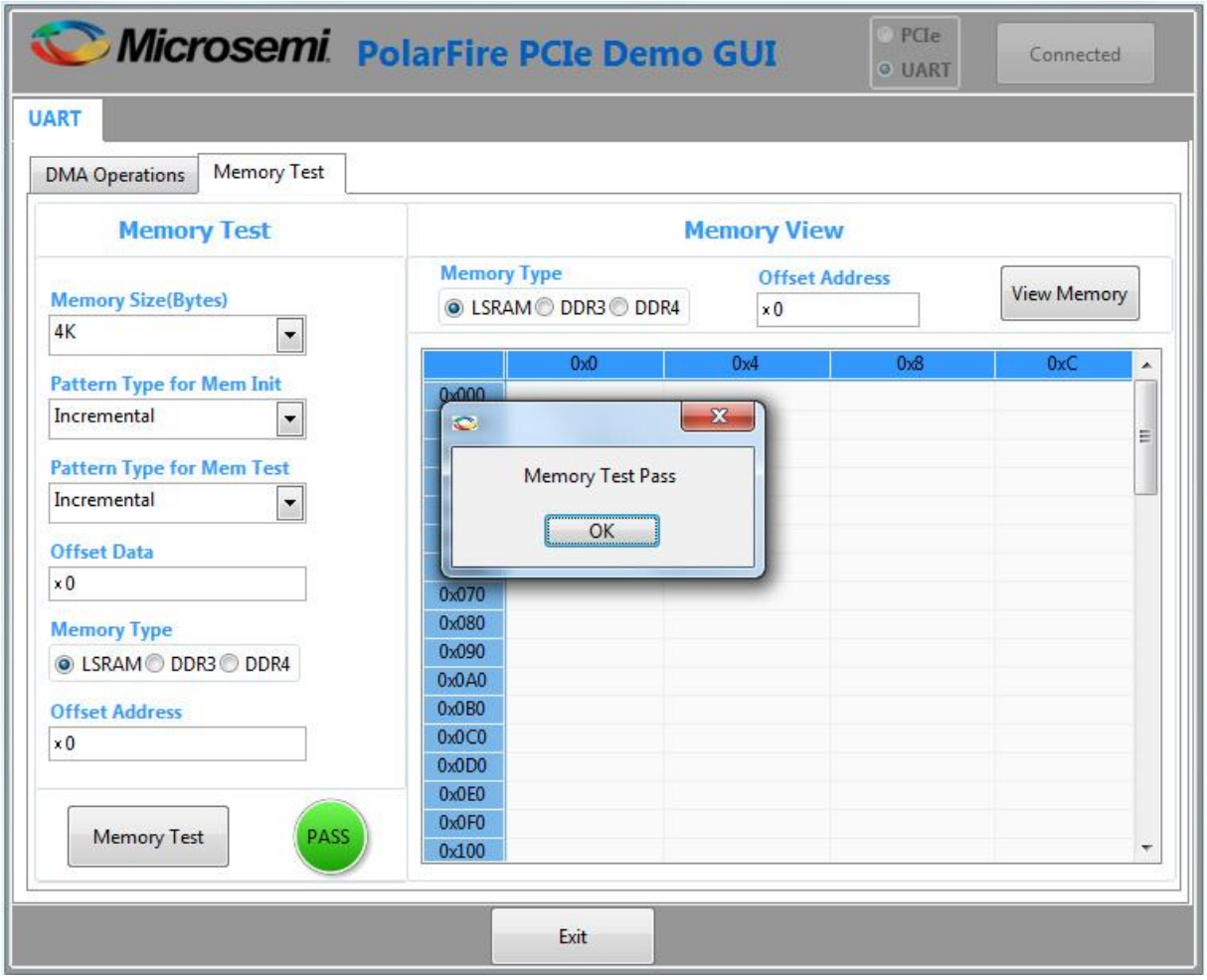


Figure 50: Demo application - UART Memory Test tab