

Everest PCIe End Point DDR3-Demo

Getting Started

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1. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.3

Updated version for Libero v2021.2

1.2 Revision 1.2

Updated version for Libero v12.4

1.3 Revision 1.1

Updated version for Libero v12.0

1.4 Revision 1.0

Revision 1.0 is the first publication of this document.

2. Getting Started

This demo design implements a PCIe end point and is based on the Microsemi[™] PCIe end point demo guide (<u>DG0756</u>). Any external PCIe root-port or bridge can establish a PCIe link and access the control registers, DDR3 16 Bit, DDR3 32 Bit, and fabric memory through the BAR space. The memory read (MRd) and write (MWr) access is done by using transaction layer packets (TLPs). These TLPs are translated by the PCIe end point into AXI4 master interface transactions and accesses the fabric memory through the CoreAXI4Interconnect IP.

The device driver on the host PC allocates memory and initiates the DMA Engine in the PolarFire PCIe controller by accessing the PCIe DMA registers through BAR0. The PCIe controller has two independent DMA Engines:

- DMA Engine 0 performs DMA from host PC memory to Everest DEV Board memory.
- DMA Engine 1 performs DMA from Everest DEV Board memory to host PC memory.

The PCIe demo application¹ uses the device driver to initiates the CoreAXI4DMA controller IP core to perform DMA between DDR3 memory and LSRAM. The two used channels of the CoreAXI4DMA controller perform the following actions:

	DMA		
DWA Channel	from	to	
0	DDR3 16 Bit	DDR3 32 Bit, LSRAM	
U	DDR3 32 Bit	LSRAM	
1	DDR3 32 Bit	DDR3 16 Bit	
I	LSRAM	DDR3 16 Bit, DDR3 32 Bit	

Table 1: CoreAXI4DMA channels actions

Beside that the PCIe demo application can initiate the CoreAXI4DMA controller through the USB UART interface on the Everest DEV Board to perform onboard transfers from and to the different memory locations, if no PCIe slot is available.

For further information please refer to the above mentioned MicrosemiTM design guide <u>DG0756</u>.

¹ <u>http://soc.microsemi.com/download/rsc/?f=mpf_dg0756_liberosocpolarfirev2p2_df</u>

2.1 Prerequisites

For the Everest PCIe End Point DDR3-Demo the following is needed:

Item	Quantity
Everest DEV Board	1
12 V / 5 A wall-mounted power adapter	1
USB 2.0 A male to mini-USB B cable for	1
UART / Programming interface to PC	
Free one-year Libero Silver software license	1
host PC with PCIe x4 slot	1

Note: The Everest DEV Board offers an on-board FlashPro5 programmer, which can be used to program and debug with Identify, SmartDebug and embedded application software using SoftConsole.

2.2 Handling the Board

Pay attention to the following points while handling or operating the board:

Handle the board with electrostatic discharge (ESD) precautions to avoid damage.

For information about ESD precautions see

https://www.microsemi.com/documentportal/doc_view/126483-esd-appnote.

2.3 Board-Setup

2.3.1 Toggle-Switch S1 – PCIe

SWITCH	PCIe LANES
S1-1 (marking)	x4
S1-2	x1

2.3.2 Toggle -Switch S5 – SC SPI-Flash enable

SWITCH	SC SPI-FLASH
S5-1 (marking)	DISABLE
S5-2	ENABLE

2.3.3 DIP-Switch S8 – FMC Voltage Selector

SWITCH	FMC VOLTAGE
S8-1 off, S8-2 off	1.8 V
S8-1 on, S8-2 off	2.5 V
S8-1 off, S8-2 on	undefined (not recommended)
S8-1 on, S8-2 on	3.3 V

2.3.4 Toggle -Switch S9 – VDDAUX2 & VDDAUX5 Voltage

SWITCH	VDDAUX2 & VDDAUX5
S9-1 (marking)	2.5 V
S9-2	FMC voltage

Figure 1: Everest Board

2.4 Powering up the Board

The Everest DEV Board is powered up using either the 12 V DC jack or the PCIe connector. For programming connect it although with your computer using USB mini B connector J9.

3. Demo Design

3.1 Prerequisites

Table 2: Software / IP Requirements

Software	Version
Libero SoC	V2021.2
Synplify Pro	R-2021.03M
FlashPro Express	V2021.2
IP	
COREAHBTOAPB3	v3.2.101
COREAXI4INTERCONNECT	v2.8.103
COREAXITOAHBL	v3.6.101
PF_CCC	V2.2.100
PF_CLK_DIV	v1.0.103
COREAXI4DMACONTROLLER	v2.0.100
CoreAHBLite	v5.5.101
CoreAPB3	v4.2.100
COREUART	v5.7.100
PF_NGMUX	v1.0.101
PF_OSC	v1.0.102
PF_INIT_MONITOR	v2.0.204
PF_TX_PLL	v2.0.300
PF_DDR3	v2.4.112
CORERESET_PF	v2.3.100
PF_SRAM_AHBL_AXI	v1.2.108
PF_TPSRAM	v1.1.108
PF_PCIE	v2.0.104
PF_XCVR_REF_CLK	v1.0.103

Before you start you have to make sure, that all cores are downloaded to your local vault.

3.2 Design Implementation

The following table lists the clock frequencies used in the design.

Table 3: Hardware Design Clock Frequencies

clock source	used by	frequency (MHz)
REF_CLK_0	CCC_111_MHz	50
CCC_111MHz	PF_DDR3_SS_0 PLL_REF_CLK,	111.111
OUT0_FABCLK_0	PF_DDR3_32Bit_0 PLL_REF_CLK,	
CCC_111MHz	PF_RESET_0 CLK,	200
OUT1_FABCLK_0	AXI4_Interconnect_0 ACLK,	
	SRAM_AXI_0 <i>ACLK</i> ,	
	CoreDMA_IO_CTRL_0 CLOCK,	
	PCIe_EP_0 AXI_CLK	
PF_DDR3_16Bit_0	AXI4_Interconnect_0 S_CLK2	166.6665
SYS_CLK,		
PF_DDR3_32Bit_0	AXI4_Interconnect_0 S_CLK4	166.6665
SYS_CLK,		

3.2.1 Top Level



Figure 2: Design Implementation – PCIe_EP_Demo (top level)

3.2.2 Smart Design PCIe_EP

Figure 3 shows the design implementation of the PCIe_EP smart design.



Figure 3: Design Implementation – PCIe_EP

The design is already fully implemented and ready to be programmed on the Everest Board. The board has to be connected with the power supply and to the PC with the USB cable. All drivers have to be installed (which should happen automatically when plugged in the first time) To program the design, there are two possibilities:

- Programming via Libero PolarFire SoC: Programming is started with the "Run PROGRAM Action" Button in the Design Flow Pane
- Programming via FlashPro Software: There is a STAPL-File ("Bitstream\PCIe_EP_Demo.stp") which can be programmed with the FlashPro Software. A new FlashPro project has to be generated and the programming file loaded into.

3.3 Configuration

3.3.1 PCle end point – ip-core PF_PCIE

Configurator				-		×
CI Express						
crosemi:SgCore:PF_PCIE:2.0.104						
General Identification Power Management I	nterrupts and Auxiliary Settings Master Settings	Slave Settings				
DCT- Ch-ll-	PCIe 0	PCIe 1				
PCIe Controller	Disabled	Enabled	-			
Number of Lanor		End Point	-			
Number of Lanes	-	X4	-			
Lane Rate		Gen2 (5.0 Gbps)	-			
		Dodiested		PF_PCI	E O	
		Dedicated			-	
Number of CDR Reference Clocks		1				
General Settings						
✓ Use embedded DLL in <u>fabric interface</u>	0		1			1
Embedded DLL Jitter Range	High					
TX PLL base data rate		5000 Mbps				-
TX PLL bit clock frequency		2500 MHz				
			i.			
Optional interfaces			1			
 Enable APB slave interface (PCIe contro Enable Dynamic Reconfiguration Interface 	ier access) :e (DRI) for XCVR lane access			PF_PC	IE	
Simulation Level Settings						
Simulation Level BFM 💌						
			\ Sym	ool /		
Messages 🔞 Errors 🗼 Warnings 🌖 Info						
ielp 🔻				ОК	Car	ncel

Figure 4: Configuration PF_PCIE - General tab

Please make sure, that embedded DLL jitter range is set to high.

User Guide

Configurator			-		×
PCI Express					
Microsemi:5gCore:PF PCIE:2.0.104					
General Identification Power Management Interrupts and Auxiliary Set	tings Master Settings Slave Settings				
	PCIe 1				
Vendor ID	0x11AA				
Sub-System Vendor ID	0x0000				
Revision ID	0x0000				
Device ID	0x1556	1	PF_PCIE_C		-1
Sub-System Device ID	0x0000				
Class Code	0x0000				
		1			
		1.			
		1			
			H-HUE		
1	L. L	Symbol /			
Log					
🔳 Messages 🔞 Errors 🗼 Warnings 🌗 Info					
Help -		ОК		Can	el

Figure 5: Configuration PF_PCIE - Identification tab

Configurator			-		×
PCI Express					
Microsemi:SgCore:PF_PCIE:2.0.104					
General Identification Power Management Interrupts and Auxiliary Se	ttings Master Settings Slave Settings				
	PCIe 1				
Number of FTS	63				
L0s Acceptable Latency	No limit				
Enable L1 Capability	Disabled	_	PF_PCI	E_0	_
L1 Acceptable Latency					
L1 Exit Latency	-				
		Symbol	94_9C	E	
Log					
🗏 Messages 🛿 Errors 🗼 Warnings 🕕 Info					_
Help -		(ж	Can	icel

Figure 6: Configuration PF_PCIE - Power Management tab

User Guide

Configurator – 🗆 🗙 **PCI Express** Microsemi:SgCore:PF_PCIE:2.0.104 General | Identification | Power Management | Interrupts and Auxiliary Settings | Master Settings | Slave Settings | PCIe 1 PHY Reference Clock Slot Slot MSI4 Interrupts Disabled Expose Wake Signal PF_PCIE_0 Full Swing Transmit Swing De-Emphasis -3.5 dB Symbol Log 🔳 Messages 🔞 Errors 🔺 Warnings 🏮 Info Help 🔻 OK Cancel

Figure 7: Configuration PF_PCIE - Interrupts and Auxiliary Settings tab

Configurator			-		×
PCI Express					
Microsemi:SgCore:PF_PCIE:2.0.104					
General Identification Power Management Interrupts and Auxi	iliary Settings Master Settings Slave Settings				
Bar 0 Table					
	PCIe 1	1			
BAR Type	64-bit prefetchable memory				
BAR Size	64 KB				
AXI Address (32 bit)	0×03000000		PF,	PCIE_0	
H Bar 1 Table					
🗄 Bar 3 lable					
Bar 4 Table					
Bar 5 Table					
		1	PT	PCIE	
			umbol /		_
Log		9	ymbor_)		
-					
Help		Γ	OK	1 0	ancel
Ticp			UK .		neer

Figure 8: Configuration PF_PCIE - Master Settings tab BAR 0

User Guide

Configurator		-		×
PCI Express				
Microsemi:SgCore:PF_PCIE:2.0.104				
	Marker Fallings Claus Collings			1
General Identification Power Management Interrupts and Auxiliary Se	ttings Master Settings Slave Settings			
🗉 Bar O Table				
Bar 1 Table				
r				
	PCIe 1			
BAR Size		PF,	_PCIE_0	_1
AXI Address (32 bit)				
🗄 Bar 2 Table				
🗉 Bar 3 Table				
🗉 Bar 4 Table				
🖽 Bar 5 Table				
	42	PT	F_PCIE	- 1
	\ sv	mbol /		
Log				
🗏 Messages 🔞 Errors 🗼 Warnings 🌐 Info				
Help •		ОК	Ca	incel

Figure 9: Configuration PF_PCIE - Master Settings tab BAR 1 (same for BAR 3 to 5)

PCI Express MicrosemitSgCore:PF_PCIE:2.0.104 General Identification Bar 0 Table Bar 1 Table Bar 2 Table Bar Stree 1 MB Axit Address (32 bit) Bar 3 Table Bar 3 Table Bar 4 Table Bar 5 Table
Hicrosemi5gCore/F_PCIE:20.104 General Identification Bar 0 Table Bar 1 Table Bar 2 Table Bar 3 Table Bar 3 Table Bar 3 Table Bar 5 Table
General Identification Power Management Interrupts and Auxiliary Settings Slave Settings B Bar 1 Table Bar 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table BAR Type 64-bit prefetchable memory BAR 3 Table Image: State 2 Table Image: State 2 Table BAR Type 64-bit prefetchable memory Image: State 2 Table Image: State 2 Table Image: State 2 Table BAR Type 64-bit prefetchable memory Image: State 2 Table Image: State 2 Table Image: State 2 Table Bar 3 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Bar 3 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table Image: State 2 Table
Bar 3 Table Bar 3 Table Bar 3 Table Bar 3 Table Bar 5 Table Bar 5 Table Bar 5 Table
Bar 1 Table Bar 2 Table BAR Type 64-bit prefit/hable memory BAR Size 1% AXI Address (32 bit) 0x1000000
Rar 2 Table BAR Type 64-bit prefict/hable memory BAR Size 1% AXI Address (32 bit) Bar 3 Table Bar 5 Table PLOTE
PCle 1 BAR Type 64bit prefet/hable memory BAR Size 1% AXI Address (32 bit) 0x1000000
PCIE 1 BAR Type 64-bit prefetchable memory BAR Size 1/M AXI Address (32 bit) 0x10000000
BAR Type 64bit prefetchable memory BAR Size 1% AXI Address (32 bit) 0x1000000
BAR Size 1% AXI Address (32 bit) 0x1000000 Bar 3 Table Bar 5 Table
Bar 3 Table Bar 5 Table Trotal
Bar 3 Table Bar 4 Table Bar 5 Table
Bar 3 Table Bar 4 Table Bar 5 Table
Bar 5 Table Trote
Bar S Table
77.XCH
Symbol /
Log
🗐 Messages 🔞 Errors 🗼 Warnings 🌐 Info
Help -

Figure 10: Configuration PF_PCIE - Master Settings tab BAR 2

User Guide

Configurator – 🗆 🗙 **PCI Express** Microsemi:SgCore:PF_PCIE:2.0.104 General | Identification | Power Management | Interrupts and Auxiliary Settings | Master Settings | Slave Settings | Slave 0 Table PCIe 1 State Disabled Size AXI Address (32 bit) PF_PCIE_0 Translation Address (64 bit) E Slave 1 Table E Slave 2 Table E Slave 3 Table E Slave 4 Table 🗄 Slave 5 Table Symbol / Log 🔳 Messages 🔞 Errors 🔺 Warnings 🏮 Info Help 🔻 OK Cancel

Figure 11: Configuration PF_PCIE - Slave Settings tab BAR 0 (same for BAR 1 to 5)

3.3.2 DDR3 controller – ip-core PF_DDR3

The configuration for both DDR3 controllers differs only in DQ width (16 for DDR3 16 Bit and 32 for DDR 32 Bit) and instance number (0 for DDR3 16 Bit and 1 for DDR 32 Bit). All other settings are the same.

General Memory Initialization	Memory Timing	Controller	Misc.
🗆 Тор			
Protocol DDR3 -			
Generate PHY only			
⊡ Clock			
Memory Clock Frequency (MHz)	666.666		
CCC PLL Clock Multiplier	6	•	
CCC PLL Reference Clock Frequency	(MHz) 111.111		
User Logic Clock Rate	QUAD	•	
User Clock Frequency	166.6665		
Topology			
		-	
Memory Format		·	
DQ Width	16	·	
SDRAM Number of Ranks	1	·	
Enable address mirroring on odd rank	s 🗖		
DQ/DQS group size	8	-	
Row Address width	16		
Column Address Width	10	_	
Bank Address Width	3	-	
Enable DM	DM	-	
	_		
Enable Parity/Alert	Г		
Enable ECC	Г		
Number of clock outputs	1	-	

Set DQ to 32 for 32 Bit DDR3

Figure 12: Configuration PF_DDR3 - General tab

User Guide

General	Memory Initiali	zation	Memory Timi	ng	Controller	Misc.
Mode R	egister 0					
Read Bu	ırst Type Sequ	uential	•			
Burst Le	ngth Fixe	d BL8	•			
Memory	CAS Latency 9					
🗆 Mode R	egister 1					
ODT Rtt	t Nominal Value	ODT Disa	bled	•		
Memory	Additive CAS Laten	cy Disabled		•		
Output	Drive Strength	RZQ/6		•		
Mode R	egister 2					
Self Ref	resh Temperature	Normal	•			
Memory	Write CAS Latency	7				
Partial A	Array Self Refresh	Full	•			
Dynamic	: ODT (Rtt_WR)	Dynamic OD)T off ▼			

Figure 13: Configuration PF_DDR3 - Memory Initialization tab

User Guide

General	Memory Initialization	Memory Timing	Controller	Misc.
Timing	parameters dependent o	on speed bin		
tRAS (r	ns) 36			
tRCD (I	ns) 13.5			
tRP (ns) 13.5			
tRC (ns	;) 49.5			
tWR (n	s) 15			
tFAW (ns) 30			
Timing	parameters dependent o	n speed bin and clocl	k frequency	
tWTR (cycles) 5	-		
tRRD (I	ns) 7.5			
tRTP (r	is) 7.5	_		
Timing	parameters dependent o	on operating condition	ı	
tREFI (us) 7.8			
Timing	parameters dependent o	n speed bin and page	e size	
tRFC (r	ns) 350			
🗆 Other 1	iming parameters			
tZQinit	(cydes)	512		
ZQ Cali	bration Type	Short 💌		
tZQCS	(cycles)	64		
tZQope	r (cycles)	256		
Enable	User ZQ Calibration Controls			
Automa	atic ZQ Calibration Period (us)	200		

Figure 14: Configuration PF_DDR3 - Memory Timing tab

User Guide

Ge	eneral Mem	ory Initializa	tion	Memory Timing)	Controller	Misc.	
Ξ	Instance Select							
	Instance Number	0 💌						Set Instance Number to 1 for
Ξ	User Interface							32 Dit DDito
	Fabric Interface	AXI4	•	[
	AXI Width	64	•					
	AXI ID Width	4		ĺ				
Ξ	Efficiency							
	Enable Activate/P	recharge loo	ok-ahead	Γ				
	Command queue	depth		3	•			
	Enable User Refre	esh Controls						
	Address Ordering			Chip-Row-Bank-	Col 🔻			
Ξ	Misc							
	Enable RE-INIT C	ontrols 🗆						
Ξ	ODT Activation 9	Settings or	n Write					
	Enable Rank0 - Ol	ото 🔽	Enable R	ank0 - ODT1 🗖				
	Enable Rank1 - Ol	ото 🗖	Enable R	ank1 - ODT1 🕅				
Ξ	ODT Activation 9	Settings or	n Read					
	Enable Rank0 - Ol	ото 🗆	Enable R	ank0 - ODT1 🗖				
	Enable Rank1 - Ol	ото Г	Enable R	ank1 - ODT1 🖵				
Figure	e 15: Configuration	on PF_DD	R3 - Con	troller tab				

General	Memory Initialization	Memory Timing	Controller	Misc.
🗆 Simulati	ion Options			
Simulatio	on Mode Fast (skip training an	d settling time) 💌		
Through	put Options			
Pipe Lini	ng 🗖			

Figure 16: Configuration PF_DDR3 - Misc. tab

3.3.3 AXI4 Interconnect – COREAXI4INTERCONNECT

Configurator	– 🗆 X
CoreAXI4Interconnect Configurator	
Microsemi:DirectCore:COREAXI4INTERCONNECT:2.8.103	
Configuration Master Configuration Slave Configuration Crossbar Configuration	<u> </u>
Bus Configuration	
Number of Masters: 3 Number of Slaves: 5	
ID Width: 4 States Width: 32	COREAXI4INTERCONNECT_0
User Width: 1	ACLK ARESETN S. CLK0 AXI4mslave1
OPTIMIZATION Configuration	-S CLK2
Optimization: C Performance C Area C User	– AXI4mslave3 – – S_CLK4 AXI4mslave4 – AXI4mmaster0 AVI3msbave0 –
OPTIMIZATION Configuration	AXI4mmaster1
Number of Threads: Max Outstanding Transactions: 1	
Slave FIFO Address Depth: 4 Slave FIFO Data Depth: 4	
DWC Address FIFO Depth Ceiling 10 Read Arbitration Enable:	
Crossbar Mode: SAMD 🔽 🚯	▼ Symbol
Help *	OK Cancel

Figure 17: Configuration COREAXI4INTERCONNECT - Configuration tab

Configurator		- 🗆 X
CoreAXI4Interconnect Co	onfigurator	
Microsemi:DirectCore:COREAXI4INTERCONNECT	:2.8.103	
Configuration Master Configuration	Slave Configuration Crossbar Configuration	<u> </u>
Master0 Configuration		
M0 Type: AXI4	M0 Data Width: 64 💌	
M0 DWC Data FIFO Depth: 16	M0 Register Slice:	COREAXI4INTERCONNECT_0
M0 Clock Domain Crossing:	M0 Read Interleaving:	
Master1 Configuration		S_CLK0
M1Type: AXI4 💌	M1 Data Width: 64 💌	S_CLK2 AXI4mslave2
M1 DWC Data FIFO Depth: 16	M1 Register Slice:	AXI4mmaster0 AXI3mslave0
M1 Clock Domain Crossing:	M1 Read Interleaving:	AXI4mmaster2
Master2 Configuration		COREAXI4INTERCONNECT
M2 Type: AXI4	M2 Data Width: 64 💌	
M2 DWC Data FIFO Depth: 16	M2 Register Slice:	
M2 Clock Domain Crossing:	M2 Read Interleaving:	▼ Symbol
Help 🔹		OK Cancel

Figure 18: Configuration COREAXI4INTERCONNECT - Master Configuration tab

Configurator						-		×
CoreAXI4Interconnec	t Configur	rator						
Configuration Master Configuration	Slave Config	uration Crossbar Configuration	1 - 2	<u> </u>				
□ Slave0 Configuration								
S0 Type:	AXI3 💌	S0 Data Width:	64 💌					
S0 DWC Data FIFO Depth:	16 💌	S0 Register Slice:	v					
S0 SLAVE Start Address (Upper 32 Bits):	0x0	S0 SLAVE Start Address (Lower 32 Bits):	0x0					
S0 SLAVE End Address (Upper 32 Bits):	0x0	S0 SLAVE End Address (Lower 32 Bits):	0xfffffff					
S0 Clock Domain Crossing:		S0 Read Interleaving:		C	OREAXI4INTERO		CT_	0
Slave1 Configuration					- ACLK			
S1Type:	AXI4 💌	S1Data Width:	64 💌	_	ARESETN A S_CLK0	XI4mslave1	6	
S1 DWC Data FIFO Depth:	16 💌	S1 Register Slice:	v		– S_CLK2 A – S_CLK2 A	XI4mslave2 XI4mslave3	5 6	
S1 SLAVE Start Address (Upper 32 Bits):	0x0	S1 SLAVE Start Address (Lower 32 Bits):	10000000		AXI4mmaster0 A AXI4mmaster1 A	XI4mslave4 XI3mslave0	E .	
S1 SLAVE End Address (Upper 32 Bits):	0x0	S1 SLAVE End Address (Lower 32 Bits):	0×1fffffff		AXI4mmaster2			
S1 Clock Domain Crossing:		S1 Read Interleaving:			COREAXI4INTER	CONNE	CI	
Slave2 Configuration								
S2 Type:	AXI4 💌	S2 Data Width:	64 💌					
S2 DWC Data FIFO Depth:	16 💌	S2 Register Slice:	v					
S2 SLAVE Start Address (Upper 32 Bits):	0x0	S2 SLAVE Start Address (Lower 32 Bits):	20000000					
S2 SLAVE End Address (Upper 32 Bits):	0x0	S2 SLAVE End Address (Lower 32 Bits):	0x2fffffff					
S2 Clock Domain Crossing:	$\overline{\mathbf{v}}$	S2 Read Interleaving:		Symb	ol /			
Help 🔻						ОК	Cance	a

Figure 19: Configuration COREAXI4INTERCONNECT - Slave Configuration tab, Slave 0 to 2

Configurator					-	
CoreAXI4Interco	nnect Config	urator				
Microsemi:DirectCore:COREAXI4	INTERCONNECT:2.8.103					
Slave3 Configuration				1		
S3 Type:	AXI4 💌	S3 Data Width:	64 💌			
S3 DWC Data FIFO Depth:	16 💌	S3 Register Slice:	v	COREAXI		ст о
S3 SLAVE Start Address (Upper	r 32 Bits): 0x0	S3 SLAVE Start Address (Lower 32 Bits)): 30000000			.0_10
S3 SLAVE End Address (Upper)	32 Bits): 0x0	S3 SLAVE End Address (Lower 32 Bits):	0x3fffffff	ARESET	N AXI4mslave1	E
S3 Clock Domain Crossing:		S3 Read Interleaving:	Γ	-s_cl.k2 -s_cl.k4	AXI4mslave2 AXI4mslave3	E
Slave4 Configuration				AXI4mr	AXI4mslave4	
S4Type:	AXI4 💌	S4 Data Width:	64 💌	AXI4mr	AXI3mslave0 naster1 naster2	E
S4 DWC Data FIFO Depth:	16 💌	S4 Register Slice:	v	COREA	(I4INTERCONNE	CT
S4 SLAVE Start Address (Upper	r 32 Bits): 0x0	S4 SLAVE Start Address (Lower 32 Bits)	+0000000			
S4 SLAVE End Address (Upper 3	32 Bits): 0x0	S4 SLAVE End Address (Lower 32 Bits):	0x4fffffff			
S4 Clock Domain Crossing:		S4 Read Interleaving:		▼ \Symbol		
Help 🔻					ОК	Cancel

Figure 20: Configuration COREAXI4INTERCONNECT - Slave Configuration tab, Slave 3 and 4

Configurator						_		×
CoreAXI4Int Microsemi:DirectCore:C		Configurato	r					
Configuration M Data Width Configuration Crossbar Data Width	aster Configuration	Slave Configuration	Crossbar Configuration					
🗆 Enable Master Wri	ite Access							
M0 access S0: 🔽	M0 access S1: 🔽	M0 access S2: 🔽	M0 access S3: 🔽					
M0 access S4: 🔽					COREAXI4INTE	RCONNE	ECT_	0
M1 access S0: 🔽	M1 access S1: 🔽	M1 access S2: 🔽	M1 access S3: 🔽		-ACLK			
M1 access S4: 🔽					-S_CLK0	AXI4mslave1 AXI4mslave2		
M2 access S0: 🔽	M2 access S1: 🔽	M2 access S2: 🔽	M2 access S3: 🔽		— S_CLK2 — S_CLK4	AXI4mslave3 AXI4mslave4		
M2 access S4: 🔽					AXI4mmaster0 AXI4mmaster1	AXI3mslave0	•	
🗆 Enable Master Rea	ad Access				AXI4mmaster2			
M0 access S0: 🔽	M0 access S1: 🔽	M0 access S2: 🔽	M0 access S3: 🔽		COREAXI4INT	ERCONNE	ECT	
M0 access S4: 🔽								
M1 access S0: 🔽	M1 access S1: 🔽	M1 access S2: 🔽	M1 access S3: 🔽					
M1 access S4: 🔽								
M2 access S0: 🔽	M2 access S1: 🔽	M2 access S2: 🔽	M2 access S3: 🔽					
M2 access S4: 🔽				-	Symbol			
Help 🔻						OK	Cano	.el

Figure 21: Configuration COREAXI4INTERCONNECT - Crossbar Configuration tab (all checkboxes are checked)

4. Running the Demo

This section describes how to install and use the Microsemi[™] PCIe Demo application. The PolarFire PCIe demo application is a simple graphic user interface (GUI) that runs on the host PC to communicate with the PolarFire PCIe end point device. It provides PCIe link status, driver information, and demo controls. The PolarFire PCIe demo application invokes the PCIe driver installed on the host PC and provides commands to the driver according to the selection made. This section also describes how to connect the kit to the Host PC PCIe Slot. If the host PC does not offer a PCIe slot, the DMA between DDR3 16 Bit, DDR3 32 Bit and LSRAM can be exercised through the USB UART interface on the Everest DEV Board.

4.1 Installing the Microemi[™] PCIe Demo Application

To install the demo application:

- Install the GUI_Installer (setup.exe) from the following design files folder: <u>mpf_dg0756_liberosocpolarfirev2p1_df</u>\GUI_Installer.
- 2. Double-click the setup.exe in the provided GUI installation (GUI_Installer\setup.exe).
- 3. Apply default options as shown in the following figure.

PolarFire_PCIe_GUI	
Destination Directory Select the primary installation directory.	
All software will be installed in the following locations. To install software into a different location, click the Browse button and select another directory.	
Directory for PolarFire_PCIe_GUI C:\Program Files (x86)\PolarFire_PCIe_Demo\	Browse
Directory for National Instruments products C:\Program Files (x86)\National Instruments\	Browse
Back Next</td <td>>> Cancel</td>	>> Cancel

Figure 22: Installing the Microsemi PCIe Demo Application

4. Click Next to start the installation.

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PolarFire_PCIe_GUI	
Start Installation Review the following summary before continuing.	
• NI-VISA 14.0.1 Run Time Support	
Click the Next button to begin installation. Click the Back button to change the installation setting	s.
Save File << Back Next >>	Cancel

Figure 23: PCIe Demo Application Installing Steps

5. Click **Finish** to complete the installation.

User Guide

PolarFire_PCIe_GUI		
Installation Complete		
The installer has finished updating your system.		
	<< Back	Next >> Finish

Figure 24: Running the Demo - Successful Installation of PCIe Demo Application

4.2 Running the demo through PCIe

This section shows how to connect the board to host PC PCIe slot, installing the PCIe drivers and running the demo application.

4.2.1 Connection the Everest DEV Board to the host PC PCIe slot

- After successful programming, power OFF the Everest DEV Board and shut down the host PC².
- Insert the Everest DEV Board in a free PCIe slot of the host PC. The slot must have at least 4 lanes. This demo is designed to work with any PCIe Gen 2 compliant slot. If the host PC does not support Gen 2 compliant slot, the demo switches to Gen 1 mode.
- 3. Power on the power supply switch **K2**³.
- 4. Power on the host PC.
- 5. After the operating system is loaded check the **Device Manager** of the host PC for the PCIe device.

² If the PC is not powered OFF, the PCIe device detection and the selection of Gen1 or Gen2 mode may fail. PCIe hor

 $^{^{\}rm 3}$ If the PC was shut down, but the power supply is not switched off, the PC may power on without manually pressing the power button.

User Guide

🚔 Device Manager	x
File Action View Help	
⊿ 🛁 w764d-test123	
⊳ 📲 Computer	
👂 👝 Disk drives	
🔈 📲 Display adapters	
DVD/CD-ROM drives	
Human Interface Devices	
⊳ · · · · · · · · · · · · · · · · · · ·	
Mice and other pointing devices	
▷ ■ Monitors	
Network adapters	
NoMachine USB Host Adapter	
▲ Other devices	
PCI Device	
Security Devices	
Sound video and game controllers	
Storage controllers	
System devices	
Universal Serial Bus controllers	
· · ·	

Figure 25: Running the Demo - Device Manager

4.2.2 Driver Installation

Perform the following steps to install the PCIe drivers on the host PC:

- Right-click PCI Device in the Device Manager and select Update Driver Software... as shown in Fehler! Verweisquelle konnte nicht gefunden werden.. To install the drivers, administrative rights are required.
- 2. In the **Update Driver Software PCle Device** window, select **Browse my computer for driver software** as shown in Figure 26.
- 3. Browse the driver's folder and click **Next** as shown in Figure 27: <u>mpf dg0756 liberosocpolarfirev2p1 df</u>\PCIe_Drivers\Win_64bit_PCIe_Driver.
- 4. The **Windows Security** dialog box is displayed. Click **Install** as shown in the following figure. After successful driver installation, a message appears. See Figure 28.



Figure 26: Driver Installation - Browse for Driver Software

G I Update Driver Software - PCI Device	×
Browse for driver software on your computer	
Search for driver software in this location:	
liberosocpolarfirev1p1_sp1_df\PCIe_Drivers\Win_64bit_PCIe_Driver	
 Include subfolders Let me pick from a list of device drivers on my computer This list will show installed driver software compatible with the device, and all driver software in the same category as the device. 	
Next Can	cel

Figure 27: Driver Installation - Browse for Driver Software cont.



Figure 28: Driver Installation - Windows Security

😡 🗕 Update Driver Software - PolarFire PCIe	x
Windows has successfully updated your driver software	
Windows has finished installing the driver software for this device:	
PolarFire PCIe	
	Close
	Close

Figure 29: Driver Installation - Successful Driver Installation

4.2.3 Running the PCIe Demo Application

The following steps describe how to run the demo design:

- Click to expand the **PolarFire PCle** device in the host PC **Device Manager** as shown in Figure 30.
- Go to All Programs > PolarFire_PCle_GUl > PolarFire_PCle_GUl. The PolarFire PCle Demo window is displayed as shown in Figure 31.
- Click Connect. The application detects and displays the information related to the connected kit such as Device Vendor ID, Device Type, Driver Version, Driver Time Stamp, Demo Type, Supported Link Width, Negotiated Link Width, Supported Speed, Negotiated Speed, Number of Bars, and BAR Address as shown in Figure 32.
- Click the Demo Controls tab to display the LED Controls⁴, DIP Switch Status⁵, and Interrupt Counters as shown in Figure 33.
- 5. Click Start LED ON/OFF Walk and Enable Interrupt Session to view the controlling LEDs and monitoring the interrupts simultaneously as shown in Figure 34.
- 6. Click the **Config Space** tab to view the details about the PCIe configuration space as shown in Figure 35.
- Click the PCIe Read/Write tab to perform read and write operations to DDR/LSRAM using BAR2 space.
- 8. Click **Read** to read the 4 KB memory mapped to BAR2 space for DDR and LSRAM as shown in Figure 36 to Figure 38.
- 9. Click the **DMA Operations** tab for different DMA operations such as DDR and LSRAM.

⁴ Because the Everest DEV Board only has 4 LEDs, there will be a little pause while the demo application turns on LED 5 to 8.

⁵ There are no DIP switches on the Everest DEV Board.

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Figure 30: Device Manager - PolarFire PCIe device detected

<u>с</u> М	icrosemi	PolarFir	e PCIe D	emo	GUI	● ○	PCIe UART	Connect	
Device Info	Demo Controls	Config Space	PCIe Read/	Nrite	DMA Opera	ations	JART		
C	Device Vendor ID				Number	of Bars 0			
	Device Type			BAR0 A	Address × 0		BAR0 Size	e(Bytes) x 0	
	Driver Version			BAR1 A	Address x 0		BAR1 Size	e(Bytes) × 0	
Dri	iver Time Stamp			DAD2 /	ddross		DAD2 Cire	(Putor)	
	Demo Type			DANZ A	address x0		DANZ SIZE	e(bytes) x0	
s	Supported Width			BAR3 A	Address x 0		BAR3 Size	e(Bytes) x 0	
N	egotiated Width			BAR4 A	Address × 0		BAR4 Size	e(Bytes) × 0	
S	upported Speed								
N	egotiated Speed			BAR5 A	Address ×0		BAR5 Size	e(Bytes) × 0	
			Exit						

Figure 31: PCIe end point demo application

Device Info	Demo Contro	ols Config Space PCle	Read/Write DMA Operations	
ľ	Device Vendor ID	0x11AA	Number of Bars	2
	Device Type	PolarFire Evaluation kit	BAR0 Address × F010000C	BAR0 Size(Bytes) x 10000
	Driver Version	6.1.7600.16385	BAR1 Address × 0	BAR1 Size(Bytes) × ()
Di	river Time Stamp	03:13:01 14/11/2017		
	Demo Type	PolarFire PCle Demo	BAR2 Address × F000000C	BAR2 Size(Bytes) x 100000
3	Supported Width	x4 (4 lanes)	BAR3 Address × 0	BAR3 Size(Bytes) × 0
N	legotiated Width	x4 (4 lanes)	PAR4 Address Y0	RARA Size(Ruter) x 0
6	Supported Speed	5 Gbps (Gen 2)	DANA Address	DAILY SIZE(BYLES)
Ν	legotiated Speed	5 Gbps (Gen 2)	BAR5 Address × 0	BAR5 Size(Bytes) × 0

Figure 32: Demo application - Device Info tab



Figure 33: Demo application - Demo Controls tab

S M	icrosemi	PolarFir	e PCIe Dem	o GUI O PCIe Connected
Device Info	Demo Controls	Config Space	PCIe Read/Write	DMA Operations
	LED Controls	DIF ON ON	P Switch Status	Interrupt Counters No of MSI Requested 4 No of MSI Allocated 4
LED 4	4	OFF OFF	OFF OFF	Interrupt Counter1
LED	7 1			Interrupt Counter3
Start L	ED ON/OFF Walk	Enable D	IP SW Session	Enable Interrupt Session Clear Interrupt Count
			Exit	

Figure 34: Demo application - Demo Controls tab - LED walk and push button interrupt count

vice Info Demo Controls	Config Space	PCIe Read/Write	DMA O	perations
Basic Advanced Extended	Capability			Configuration Description
Туре 0	Configuration Set	tings		
Descriptor Name	Offset (0x)	Value(0x)	*	
Vendor ID	0x000	0x11AA		
Device ID	0x002	0x1556		
Command	0x004	0x506		
Status	0x006	0x10		
Revision ID	0x008	0x0		
Class Code	0x009	0x0		
Cache Line Size	0x00C	0x10		
Latency Timer	0x00D	0x0		
Header Type	0x00E	0x0	=	
BIST	0x00F	0x0		
Base Address 0	0x010	0xE010000C		
Base Address 1	0x014	0x0		
Base Address 2	0x018	0xE000000C		
Base Address 3	0x01C	0x0		
Base Address 4	0x020	0x0		
Base Address 6	0x024	0x0		
Expansion ROM Base Address	0x028	0x0		
Subsystem Vendor ID	0x02C	0x0		
Subsystem ID	0x02E	0x0		
Capabilities PTR	0x034	0x80	-	-

Figure 35: Demo application - Config Space tab

Device Info	Demo Controls	Config Space	PCIe Read/Write	DMA Operations	
PCIe-BA	R2-LSRAM 🔘 PC	Ie BAR2-DDR3	O PCIe-BAR2-DE	PCIe DDR C)ffset Address ×0
	0x0		0x4	0x8	0xC
0x000	400		3FF	3FE	3FD
0x010	3FC		3FB	3FA	3F9
0x020	3F8		3F7	3F6	3F5
0x030	3F4		3F3	3F2	3F1
0x040	3F0		3EF	3EE	3ED
0x050	3EC		3EB	3EA	3E9
0x060	3E8		3E7	3E6	3E5
0x070	3E4		3E3	3E2	3E1
0x080	3E0		3DF	3DE	3DD
0x090	3DC		3DB	3DA	3D9
0x0A0	3D8		3D7	3D6	3D5
0x0B0	3D4		3D3	3D2	3D1
0x0C0	3D0		3CF	3CE	3CD
0x0D0	3CC		3CB	3CA	3C9
0x0E0	3C8		3C7	3C6	3C5
0x0F0	3C4		3C3	3C2	3C1
0x100	3C0		3BF	3BE	3BD
0x110	3BC		3BB	3BA	3B9
0x120	3B8		3B7	3B6	3B5
Read Pr	ogress				Read

Figure 36: Demo application - PCle Read/Write tab – LSRAM

S N	licrosemi.	PolarFir	e PCIe Dem	o GUI	PCIe UART
Device Into	Demo Controls	Config Space	PCIe Read/ Write	DMA Operations	
PCIe-BA	R2-LSRAM	CIe BAR2-DDR3	PCIe-BAR2-DDF	PCIe DDR (Offset Address ×0
	0x0		0x4	0x8	0xC 🔺
0x000	400		3FF	3FE	3FD ≡
0x010	3FC		3FB	3FA	3F9
0x020	3F8		3F7	3F6	3F5
0x030	3F4		3F3	3F2	3F1
0x040	3F0		3EF	3EE	3ED
0x050	3EC		3EB	3EA	3E9
0x060	3E8		3E7	3E6	3E5
0x070	3E4		3E3	3E2	3E1
0x080	3E0		3DF	3DE	3DD
0x090	3DC		3DB	3DA	3D9
0x0x0	3D8		3D7	3D6	3D5
0x0B0	3D4		3D3	3D2	3D1
0x0C0	3D0		3CF	3CE	3CD
0x0D0	3CC		3CB	3CA	3C9
0x0E0	3C8		3C7	3C6	3C5
0x0F0	3C4		3C3	3C2	3C1
0x100	3C0		3BF	3BE	3BD
0x110	3BC		3BB	3BA	3B9
0x120	3B8		3B7	3B6	3B5 T
Read Pr	rogress				Read
			Exit		

Figure 37: Demo application - PCle Read/Write tab - DDR3 16 Bit

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Everest PCIe End Point DDR3 Demo

evice Info	Demo Controls	Config Space	PCIe Read/Write	DMA Operations	
PCIe-BA	R2-LSRAM OP	Cle BAR2-DDR3	PCIe-BAR2-DD	PCIe DDR	Offset Address ×0
	0x0		0x4	0x8	0xC
0x000	400		3FF	3FE	3FD
0x010	3FC		3FB	3FA	3F9
0x020	3F8		3F7	3F6	3F5
0x030	3F4		3F3	3F2	3F1
0x040	3F0		3EF	3EE	3ED
0x050	3EC		3EB	3EA	3E9
0x060	3E8		3E7	3E6	3E5
0x070	3E4		3E3	3E2	3E1
0x080	3E0		3DF	3DE	3DD
0x090	3DC		3DB	3DA	3D9
0x0x0	3D8		3D7	3D6	3D5
0x0B0	3D4		3D3	3D2	3D1
0x0C0	3D0		3CF	3CE	3CD
0x0D0	3CC		3CB	3CA	3C9
0x0E0	3C8		3C7	3C6	3C5
0x0F0	3C4		3C3	3C2	3C1
0x100	3C0		3BF	3BE	3BD
0x110	3BC		3BB	3BA	3B9
0x120	3B8		3B7	3B6	3B5
Read Pr	ogress				Read

Figure 38: Demo application - PCle Read/Write tab - DDR3 32 Bit

4.2.3.1 Continuous DMA Operations

The following instructions describe running DMA operations between PC and DDR3 16 Bit, PC and DDR3 32 Bit and PC and LSRAM:

- Select one of the following options from the DMA Transfer Type Selection drop-down list:
 - PC->DDR3 to transfer data from host PC to DDR3 16 Bit memory
 - DDR3->PC to transfer data from DDR3 16 Bit memory to host PC
 - Both: PC<->DDR3 to transfer data from host PC to and from DDR3 16 Bit memory
 - PC->DDR4 to transfer data from host PC to DDR3 32 Bit memory
 - DDR4->PC to transfer data from DDR3 32 Bit memory to host PC
 - Both PC<->DDR4 to transfer data from host PC to and from DDR3 32 Bit memory
 - PC->LSRAM to transfer data from host PC to LSRAM memory
 - LSRAM->PC to transfer data from LSRAM memory to host PC
 - Both: PC<->LSRAM to transfer data from host PC to and from LSRAM memory

- Select Transfer Size⁶ (4 KB to 64 KB) from the drop-down list. Maximum contiguous DMA size is 64 KB because the host PC may not have contiguous memory of more than 64 KB. For DMA operations that require more than 64 KB, use SGDMA.
- 3. Enter the Loop Count in the box.
- 4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows Continuous DMA Operations.

C Microsemi. Pol	arFire PCIe Demo GUI	PCIe Connected
Device Info Demo Controls Config	g Space PCIe Read/Write DMA Opera	ations
PCIe Continuous DMA PCIe SGDMA Fr	abric Core DMA	
Operations Memory Test		
DMA Transfer Type Selection PC->LSR/ PC to LSRAM ✓ PC->L PC to LSRAM Both F Transfer Size(Bytes) 4K ▼ Throughput(MBps) 0 DDR3 Both F PC->E DDR3	AM	
Loop Count 1 Start T	Fransfer PC to LSRA PC to LSRAM A Exit	1 2 No of DMA Transfers AM Image: State of the

Figure 39: Demo application - continuous DMA operations

⁶ The AXI LSRAM in the design is configured for 4 kB. This 4 kB is over written if more than 4 kB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

Device Info	Demo (Controls	Config S	pace PC	Ie Read/	Write	OMA Ope	rations			
PCIe Continuo	us DMA	PCIe SGD	MA Fabr	ic Core DM	A						
Operations	Memory	Test									
DMA Tra Selectio	ansfer Typ n	e E	loth PC<->	SRAM	•	1160 -				+ 👤	們
PC to	LSRAM		LSR/	M to PC		1150 -	\square			\wedge	
Transfer Si	ze(Bytes)	64K 💌	Transfer Si	ze(Bytes)	64K 🖵	1140- (1130- 1120-	/		~~/		
Through	nput(MBps	5) 1080	Through	put(MBps) 1130	ndyfonor 1100-					
Avg Thru	uput(MBps	5) 1086	Avg Thr	iput(MBps	5) 1135	1090 -	\checkmark		$\overline{}$		
Loop Co	unt 10		Start Trar	sfer		1070 - 1	2	3 4 5 No of Di	6 7 AA Transfers	8 9	10
						PC t	PC to LSP		LSRA	M to PC	^

The following figure shows the throughput and average throughput in MBps.

Figure 40: Demo application - continuous DMA from PC to LSRAM and vice versa

4.2.3.2 Continuous DMA - Memory Test

The following instructions describe running **Memory Test** between PC and DDR3 16 Bit, DDR3 32 Bit and LSRAM:

- 1. Select one of the following options from the Test Selection drop-down list:
 - PC<->DDR3 to transfer data from host PC to and from DDR3 16 Bit memory
 - PC<->DDR4 to transfer data from host PC to and from DDR3 32 Bit memory
 - **PC<->LSRAM** to transfer data from host PC to and from LSRAM memory
- 2. Select Transfer Size (4 kB to 64 kB) from the drop-down list.
- 3. Select **Pattern Selection** from the drop-down list (Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's).
- 4. Click Start. GUI performs the following task:
 - The host PC creates a buffer and initializes the memory
 - Initiates the PC to DDR DMA
 - Erases the PC buffer

- Initializes the DDR to PC DMA
- · Compares the memory against expected memory

The following figure shows Continuous DMA - Memory Test tab.

vice Info Demo	Controls	Config Space	PCIe Read	I/Write DN	IA Operations		
Te Continuous DMA	PCIe SGDI	MA Fabric Co	re DMA				
Operations Memory	y Test						
Memory Te	st			View	Memory		
Test Selection		Address Of	fset ×0		View Memory		
✓ PC<->DDR3 PC<->DDR4 PC<->LSRAM 4K Pattern Selection Increment Start		0x0 0x10 0x20 0x30 0x40 0x50 0x60 0x70 0x80 0x90 0x40 0x80 0x80 0x20	0x0	0x4		0xC	
		0xD0 0xE0					-

Figure 41: Demo application – Continuous Memory Test – Transfer Type Selection

Memory Test Successful window appears, as shown in the following figure.

Device Info Demo	Controls Co	nfig Space	PCIe Read/	Write DMA Op	erations		
PCIe Continuous DMA	PCIe SGDMA	Fabric Cor	e DMA				
Operations Memor	y Test						
Memory Te	st			View Men	ıory		
Test Selection		Address Off	set ×0		View Memory		
PC<->DDR3	•				0.2	0vC	
6 8		0-0		X	3	A	Ê
T (C ())					7	8	1.00
Transfer Size (Byte	esj	0x20 Memory Test Successfull		uccessfull	B	c	
64K 👻		0x30			F	10	_
	-1.5	0x40			13	14	_
Datters Colortion		0x50	13	10	17	18	
Fattern Selection		0x60	19	1A	1B	1C	
Increment		0x70	1D	1E	1F	20	
80		0x80	21	22	23	24	
		0x90	25	26	27	28	
2		0xA0	29	2A	2B	2C	
Start		0xB0	2D	2E	2F	30	
		0xC0	31	32	33	34	
		0xD0	35	36	37	38	
		0.50	20	20	28	20	

Figure 42: Demo application - Continuous DMA Memory Test - Memory Test Successful

If memory test fails, the GUI displays the first failed memory location. Change the **Offset Address** and click **View Memory** to read the RAM memory content.

4.2.3.3 SGDMA Operations

The following instructions describe running SGDMA operations between PC and DDR3 16 Bit, PC and DDR3 32 Bit:

- Select one of the following options from the DMA Transfer Type Selection drop-down list:
 - PC -> DDR3 to transfer data from host PC to DDR3 16 Bit memory
 - DDR3 -> PC to transfer data from DDR3 16 Bit memory to host PC
 - Both: PC <-> DDR3 to transfer data from host PC to and from DDR3 16 Bit memory
 - PC -> DDR4 to transfer data from host PC to DDR3 32 Bit memory
 - DDR4 -> PC to transfer data from DDR3 32 Bit memory to host PC
 - Both: PC <-> DDR4 to transfer data from host PC to and from DDR3 32 Bit memory

- 2. Select Transfer Size (4 kB to 64 kB) from the drop-down list.
- 3. Enter the **Loop Count** in the box. The **Buffer Descriptors** show the number of descriptors created by the host driver for each SGDMA operation.
- 4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows the SGDMA Operations.

C Microsemi	PolarFire PC	e Dem	o GUI	PCIe UART	Connected
Device Info Demo Controls	Config Space PCIe R	lead/Write	DMA Operations		
PCIe Continuous DMA PCIe SGI	MA Fabric Core DMA				
Operations Memory Test					
DMA Transfer Type	PC->DDR4	550			+ 💌
Selection	✓ PC->DDR4	500			
PC to DDR4	DDR4->PC	450			
	PC->DDR3	400			
Transfer Size(Bytes)	DDR3 -> PC	350 ·			
Throughput(MBps) 0	Both PC<->DDR3	¥ 300·			
Avg Thruput(MBps) 0	Avg Thruput(MBps) 0	250-			
Buffer Descriptors 0	Buffer Descriptors 0	150 · 100 ·			
	1	50			
		0			
Loop Count 1	Start Transfer		No of	I DMA Transfers	2
			PC to DDR4		R4 to PC
			PC to DDR4 Avg 🖊	DDR4 to	o PC Avg 🔼
	E	xit			

Figure 43: Demo application - SGDMA operations

4.2.3.4 SGDMA Memory Test

The following instructions describe running **Memory Test** between PC and DDR3 16 Bit, DDR3 32 Bit and LSRAM:

- 1. Select one of the following options from the Test Selection drop-down list:
 - PC <-> DDR3 to transfer data from host PC to and from DDR3 16 Bit memory
 - PC <-> DDR4 to transfer data from host PC to and from DDR3 32 Bit memory
- 2. Select Transfer Size (4 kB to 1 MB) from the drop-down list.
- 3. Select **Pattern Selection** from the drop-down list (Increment, Decrement, Random, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's).

- 4. Click Start. GUI performs the following task:
 - The host PC creates a buffer and initializes the memory
 - Initiates the PC to DDR DMA
 - Erases the PC buffer
 - Initializes the DDR to PC DMA
 - Compares the memory against expected memory
- 5. Click OK.
- 6. Change the **Offset Address** and click **View Memory** to read the RAM memory content.

The following figure shows SGDMA Memory Test tab.

🔍 Microsem	PolarFire PCIe Demo GUI	
Device Info Demo Controls	Config Space PCIe Read/Write DMA Operations	
PCIe Continuous DMA PCIe SG	MA Fabric Core DMA	
Operations Memory Test		_
Memory Test	View Memory	
Test Selection	Address Offset ×0 View Memory	
PC<->DDR3 ▼ ✓ PC<->DDR3 PC<->DDR4 Increment ▼ Transfer Size (Bytes) 4K ▼	0x0 0x4 0x8 0xC 0x0	
	Exit	

Figure 44: Demo application - SGDMA Memory Test tab

Memory Test Successful window appears, as shown in the following figure.

evice Info Demo Contr	ols Config Spa	ce PCIe Read/	Write DMA Ope	rations					
PCIe Continuous DMA PCIe	SGDMA Fabric	Core DMA							
Operations Memory Test]								
Memory Test		View Memory							
Test Selection	Addr	ess Offset ×0	Vi	ew Memory					
			x	0x8	0xC				
	0x0			3	4	H			
	0x10	Memory Test S	Successfull	7	8				
Pattern Selection	0x20	0x20 0x30 OK		В	С				
Increment 👻	0x30			F	10				
	0x40			13	14				
Transfer Size (Bytes)	0x50	C1	10	17	18				
1MB 👻	0x60	19	1A	18	1C				
	0x70	1D	1E	1F	20				
	0x80	21	22	23	24				
	0x90	25	26	27	28				
Start	0xA0	29	ZA	ZB	20				
	0xB0	2D	2E	2F	30				
	0xC0	31	32	33	34				
	0xD0	35	36	37	38				
	0xE0	39	3A	3B	3C	*			

Figure 45: Demo application - SGDMA Memory Test Successful

4.2.3.5 Core DMA Operations

The following instructions describe running DMA operations between LSRAM and DDR3 16 Bit, LSRAM and DDR3 32 Bit, DDR3 16 Bit and DDR3 32 Bit:

- Select one of the following options from the DMA Transfer Type Selection drop-down list:
 - LSRAM -> DDR3 to transfer data from LSRAM to DDR3 16 Bit memory
 - DDR3 -> LSRAM to transfer data from DDR3 16 Bit memory to LSRAM
 - Both: LSRAM <-> DDR3 to transfer data from LSRAM to and from DDR3 16 Bit memory
 - LSRAM -> DDR4 to transfer data from LSRAM to DDR3 32 Bit memory
 - DDR4 -> LSRAM to transfer data from DDR3 32 Bit memory to LSRAM
 - Both: LSRAM <-> DDR4 to transfer data from LSRAM to and from DDR3 32 Bit memory
 - DDR4 -> DDR3 to transfer data from DDR3 32 Bit to DDR3 16 Bit memory
 - DDR3 -> DDR4 to transfer data from DDR3 16 Bit to DDR3 32 Bit memory

- Both: DDR4 <-> DDR3 to transfer the data from DDR3 32 Bit to and from DDR3 16 Bit memory
- 2. Select **Transfer Size**⁷ (4 kB to 1 MB) from the drop-down list.
- 3. Enter the Loop Count in the box.
- 4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows Core DMA Operations.
- 5. Click **Exit** to quit the demo.

C Microsemi	PolarFire PCIe Demo GUI
Device Info Demo Controls	Config Space PCIe Read/Write DMA Operations
PCIe Continuous DMA PCIe SGI	MA Fabric Core DMA
Operations	
DMA Transfer Type Selection	DDR4->LSRAM ▼ 550 - 550 - 500
DDR4 to LSRAM Transfer Size(Bytes) 4K • Throughput(MBps) 0	LSRAM->DDR4 450 - Both LSRAM<->DDR4 400 - DDR3->LSRAM 400 - LSRAM ->DDR3 350 - Both LSRAM<->DDR3 300 - DDR3->DDR4 250 - DDR4->DDR3 200 -
Avg Inruput(MBps) 0	Avg Inruput(MBps) 0 150 - 100 - 50 -
Loop Count 1	Start Transfer No of DMA Transfers DDR4 to LSRAM Mark LSRAM to DDR4 Avg
	Exit

Figure 46: Demo application - Core DMA operations

⁷ The AXI LSRAM in the design is configured for 4 kB. This 4 kB is over written if more than 4 kB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

4.3 Running the demo through UART

If no PCIe slot is available, onboard DMA and memory test could be done by the demo application using the USB UART interface of the Everest DEV Board. The COM port number of the USB UART interface will be set by the operating system after installation. Checking the COM ports with the **Device Manager** will give a similar result like in the following figure.

Ports (COM & LPT)
 FlashPro5 Port (COM10)
 FlashPro5 Port (COM11)
 FlashPro5 Port (COM8)
 FlashPro5 Port (COM9)

Figure 47: Device Manager - COM ports

The following steps describe how to run the reference design using the USB UART interface:

- Go to All Programs > PolarFire_PCle_GUl > PolarFire_PCle_GUl. The PolarFire PCle Demo window is displayed as shown in Figure 48.
- 2. Select the **UART** radio button and click **Connect**. The GUI application scans for UART port and after successful connection, displays the DMA Operations UART tab as shown in Figure 49, page 48.

S M	icrosemi	PolarFire	e PCIe De	emo Gl	UI 🖁	D PCIe D UART	Connect
Device Info	Demo Controls	Config Space	PCIe Read/W	rite DMA	Operations	UART	
D	evice Vendor ID			Ν	Number of Bars (D	
	Device Type		E	BAR0 Addres	s ×0	BAR0 Size(By	tes) x 0
	Driver Version			BAR1 Addres	s x 0	BAR1 Size(By	tes) x ()
Dri	iver Time Stamp						
	Demo Type			BAR2 Addres	s × O	BAR2 Size(By	tes) x 0
S	upported Width			BAR3 Addres	5 x 0	BAR3 Size(By	tes) x0
N	egotiated Width			BAR4 Address	s ×0	BAR4 Size(By	tes) ×0
s	upported Speed						
N	egotiated Speed		E	BAR5 Addres	s ×0	BAR5 Size(By	tes) ×0
			(
			Exit				

Figure 48: PCIe end point demo application

ARI										
MA Operations	Memory Test									
Continous D Type Selecti	MA Transfer	DDR4->LSRAM	500						4	æ
DDR4 to LSI	RAM	✓ DDR4->LSRAM LSRAM->DDR4 Both DDR4<->LSRAM	450 400							
Transfer Size(B	ytes) 4K 💌	DDR3->LSRAM LSRAM->DDR3 Both DDR3<->LSRAM	(sd 350 300							
Throughput(M	Bps) 0	DDR3->DDR4 DDR4->DDR3 Both DDR3<->DDR4	1 1 250							
Avg Thruput(M	Bps) 0	Avg Thruput(MBps) 0	≓ 150 100							
		 ~ **	50	-						
Loop Count	1	Start Transfer		1 2	3	4 5 No of D	6 MA Trai	nsfers	9	10 11
			DDF	DDR4 t R4 to LSI	o LSRAI RAM Av	м 🖳 g 🔼	LSRAN	SRAM to 1 to DD	DDR R <mark>4 Av</mark>	4 📥 9 🔼

Figure 49: Demo application - UART DMA operations

The following instructions describe the different ways to read data through LSRAM and DDR:

- 1. Select one of the following options from the Continuous DMA Transfer Type Selection drop-down list:
 - DDR3 -> LSRAM transfer data from DDR3 16 Bit to LSRAM memory.
 - LSRAM -> DDR3 transfer data from LSRAM to DDR3 16 Bit memory.
 - Both: DDR3 <-> LSRAM transfer data from DDR3 16 Bit to and from LSRAM memory.
 - LSRAM -> DDR4 transfer data from LSRAM to PolarFire DDR3 32 Bit memory.
 - **DDR4 -> LSRAM** to transfer data from DDR3 32 Bit to LSRAM memory.
 - Both: LSRAM <-> DDR4 transfer data from LSRAM to and from DDR3 32 Bit memory.
 - **DDR4 -> DDR3** transfer data from DDR3 32 Bit to DDR3 16 Bit memory.
 - DDR3 -> DDR4 transfer data from DDR3 16 Bit to DDR3 32 Bit memory.
 - Both: DDR4 <-> DDR3 transfer data from DDR3 32 Bit to and from DDR3 16 Bit memory.

- Both: DDR3 <-> DDR4 transfer data from DDR3 16 Bit to and from DDR3 32 Bit memory.
- 2. Select **Transfer Size**⁸ (4 kB to 512 kB) from the drop-down lists.
- 3. Enter the Loop Count in the box.
- 4. Click **Start Transfer**. After a successful DMA operation, the GUI displays the throughput and average throughput in MBps. The following figure shows DMA throughput and average throughput from the DDR memory to the LSRAM.

The following instructions describe running **Memory Test** between PC and DDR3 16 Bit, DDR3 32 Bit and LSRAM:

- 1. Select **Transfer Size** (4 kB to 1 MB) from the drop-down list.
- Select Pattern Selection from the drop-down list (Increment, Decrement, Fill with Zeros, Fill with Ones, Fill with all A's, and Fill with all 5's). For successful Memory test operation, the Patter Type for Mem Init and Patter Type for Mem Test should be same.
- 3. Click Memory Test.
 - GUI sends command to fabric logic to initiate the LSRAM, DDR3 16 Bit and DDR3 32 Bit memory.
 - GUI sends command to fabric logic to read and compare LSRAM, DDR3 16 Bit and DDR3 32 Bit memory.
- 4. Click **View Memory**. It shows 1 kB of RAM memory content.
- 5. Click OK.
- 6. Change the **Offset Address** and click **View Memory** to read the RAM memory content.
- 7. Click **Exit** to quit the demo.

⁸ The AXI LSRAM in the design is configured for 4 kB. This 4 kB is over written if more than 4 kB of DMA operation is performed on LSRAM. This option is provided to exercise the throughputs with larger DMA size.

The following figure shows the UART Memory Test tab.

ART Microsemi. Po	olarFire PCIe Demo	GUI	○ PCIe○ UART	Connected
DMA Operations Memory Test Memory Test	Me	emory View	1	
Memory Size(Bytes)	Memory Type SRAM DDR3 DDR4	Offset Ac	ldress	View Memory
Pattern Type for Mem Init Incremental Pattern Type for Mem Test Incremental Offset Data x0 Memory Type ISRAM DDR3 DDR4 Offset Address x0	0x0 0x000 0x000 0x070 0x070 0x080 0x090 0x080 0x090 0x080 0x080 0x080 0x080 0x020 0x0E0 0x0F0		Uxă	UxC E

Figure 50: Demo application - UART Memory Test tab